HMT7748 GENIE IO-Link DEVICE DUAL PHY

The HMT7748 GENIE family IC provides a bridge between a microcontroller with a sensor or actuator function and a 24V supply and signalling cable, specified to support IO-Link.

[1] This specification makes reference to IO-Link Interface and System Specification Version 1.1, November 2010

1.1 Features

- integrated UART peripheral with M-sequence handling (inc. checksum) for all IO-Link sequences to specification 1.1
- single octet UART mode for unlimited M-sequence size and continuous data transfer
- internal data buffer for up to 15 octets
- transparent UART mode for special applications
- quartz-free IO-Link clock extraction and timing generation at 38.4kBaud and 230.4kBaud
- dual outputs independently configured to be high-side, low-side or push-pull (<10Ω)
- configurable output doubling for additional drive strength requirements (nom. 500mA)
- optional direct control of the DIO channel
- fast switching time (<1µs)
- configurable short circuit current limit and reporting
- zener limits for rapid inductive load switch off
- 5V to 35V supply range
- 5V and 3.3V, 50mA linear regulators
- Software controlled 5V linear regulator power-down mode
- configurable frequency & voltage (5V-10.5V), 50mA DCDC regulator
- software controlled DCDC sleep mode
- internal reverse polarisation diode (DOUT pin)
- full zero current reverse polarity protection
- over-voltage protection to 35V
- configurable under-voltage detection
- ESD protection to 4kV
- EMC surge protection to IEC 60255-5 (2A/50µs)
- configurable thermal shutdown levels
- 7-bit, calibrated, temperature measurement
- two configurable current mode LED outputs
- small format 4mm x 4mm, 20LD QFN package

In normal operation the HMT7748 is configured by the microcontroller via the SPI interface at start-up. Typically the HMT7748 then operates as a Single Input Output IO-Link device driving the output lines as configured by the microcontroller. If the device is connected to an IO-Link master, then the master can initiate communication and exchange data with the microcontroller while the HMT7748 acts as the physical/datalink layer for the communication.

This datasheet is subject to change without notice. Please check HMT website for latest version.

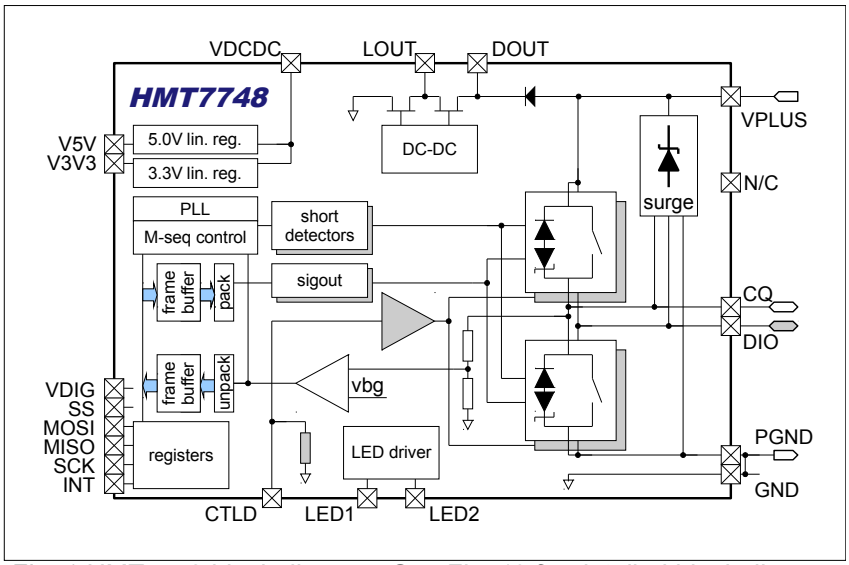


Fig. 1 HMT7748 block diagram. See Fig. 19 for detailed block diagram

2 Package and pin-out

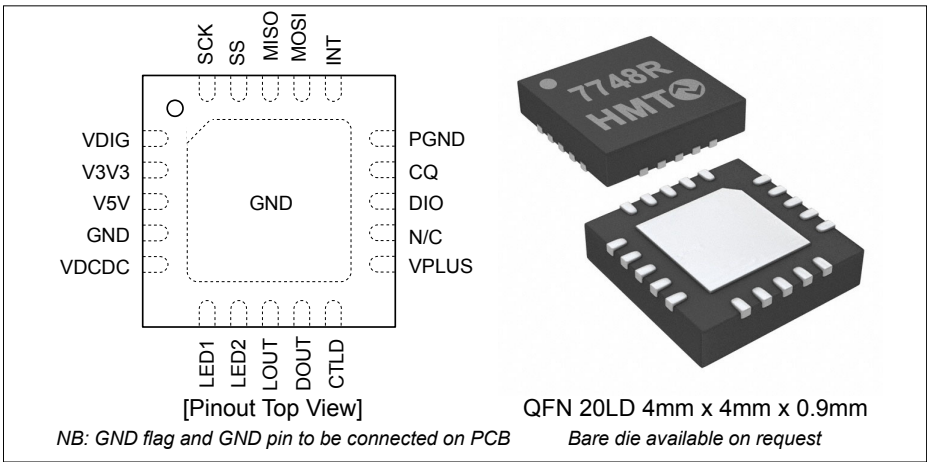


Fig. 2: Package and pinout

3 Example Applications

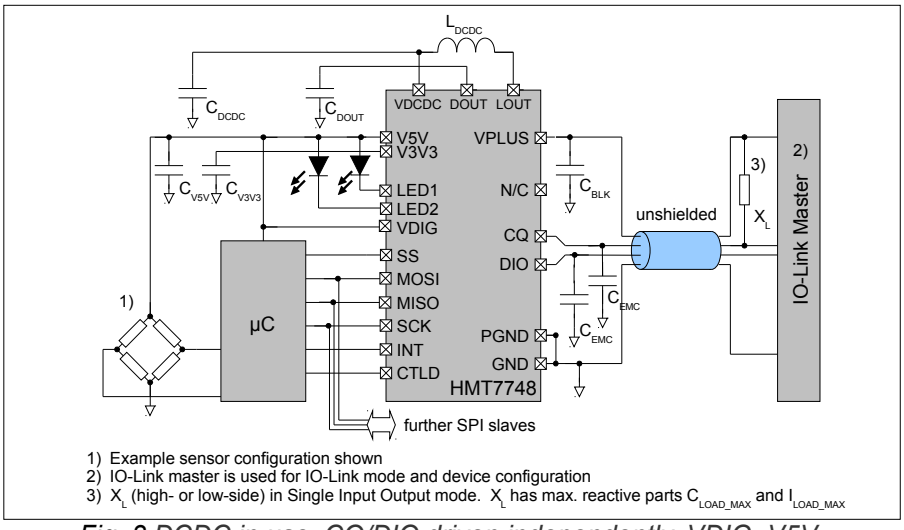


Fig. 3 DCDC in use, CQ/DIO driven independently, VDIG=V5V

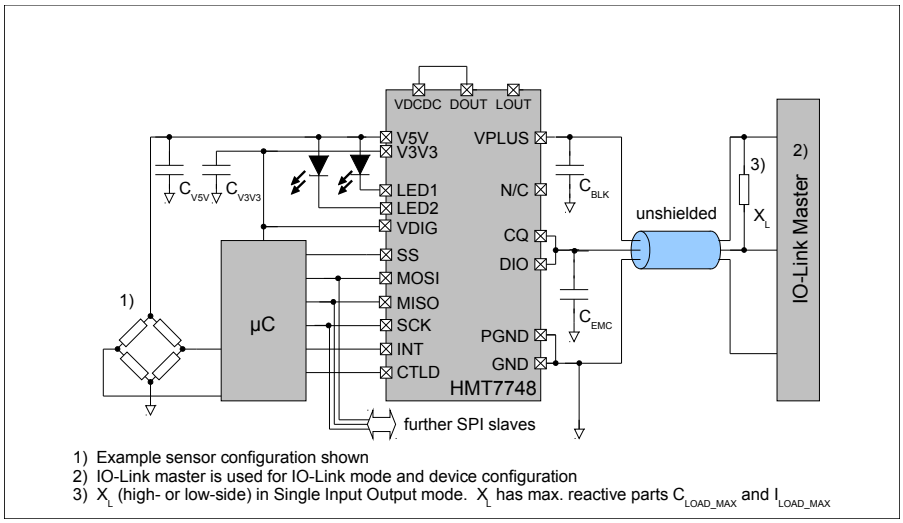


Fig. 4 DCDC bypassed, CQ/DIO driven in JOIN mode, VDIG=V3V3

4 Start-up

At start-up, power is applied via the cable on VPLUS. A Power-On-Reset (POR) circuit ensures correct start-up of the HMT7748, and that the output switches are initially in a high impedance state. The device core of the HMT7748, including the control for the 5V regulator, is supplied by the V3V3 supply.

The SPI communication logic is reset whenever SS='1' and is independent of the HMT7748 power on reset itself. It is therefore possible to read the SPI register values even when the HMT7748 is in reset. In particular, the STATUS:RST bit is read as part of the STATUS byte on every SPI access. This bit is cleared when the device is in reset, or when the device has been reset. This status information can be used as set out in Table 1 to determine the HMT7748 reset state, and also to react to unexpected reset conditions.

Device state	STATUS:RST	INT	comment
Power-On-Reset (POR)	0	0	HMT7748 is in power on reset (checked at the start of the SPI access). Only the STATUS:RST bit is valid. The microcontroller may wait for a high level on INT before proceeding.
device reset (post POR)	0	1	HMT7748 has been reset, and the INT line is forced high. Write STATUS:RST='1' to allow normal operation of the HMT7748.
operation	1	x	normal operation

Table 1 HMT7748 Reset conditions

The microcontroller should initialise the state of the internal registers to the desired values after reset.

5 SPI Communication

Internal registers are provided to observe and control the HMT7748 state. These register settings are read and written via the SPI interface, where the HMT7748 is the SPI slave. The operating voltage level for inputs and outputs on the SPI interface is set by the VDIG pin. This pin will typically be directly connected either to the V5V or V3V3 supplies.

The detailed timing diagram is shown in Fig. 5. Data is shifted into an internal shift register from input MOSI on each rising SCK edge. Data is made available on pin MISO at each falling SCK edge. Note that the MISO line is only driven when the slave specific select line SS='0', which allows other SPI slaves to share the same SPI bus.

The MSB of the address byte is a WR/RDn bit, where a '1' indicates that each byte will be written to the registers. Valid data is always made available on the MISO line independent of the WR/RDn bit. Where a register is written and read in the same operation, then the read value will be the old register value. During read operations, the level of the MOSI line is ignored for the data bytes.

The byte sequence for data transmission is shown in Fig. 6. Each transmission sequence consists of a falling SS edge which synchronises transmission, followed by a target register address byte. During the transmission of the address byte from the microcontroller to the HMT7748, the status register contents are sent from the HMT7748 to the microcontroller.

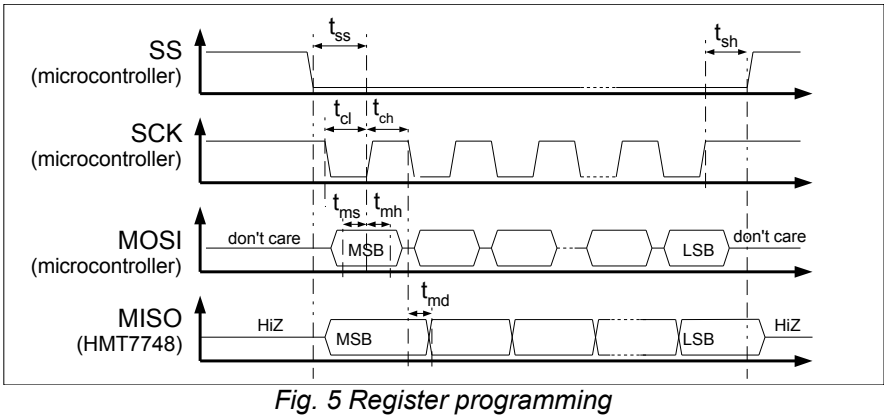


Fig. 5 Register programming

5.1 Multiple byte exchange

Multiple registers at consecutive addresses can be read or written by extending the access as shown in Fig. 6. Bytes are written on the rising SCK clock edge of the eighth bit of each byte.

With the WR/RDn bit set, a simultaneous read/write operation is started. Now, with a multiple byte exchange, it is

possible to both read and write the values of multiple register bytes in one operation. This is particularly useful with larger M-sequence types where there is limited time available for the SPI exchange.

The STATUS of the HMT7748 will always be transmitted as the first response byte on the MISO line.

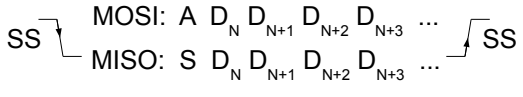
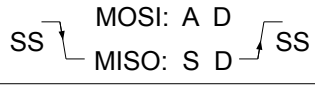
Consecutive access	
Single access	
Key: *A: Address byte, D: Data byte, S: Status byte*	

Fig. 6: Single byte and sequential byte accesses

6 DIO Pin

The DIO pin may be operated in one of two modes:

- DIO mode: If the DCTL:DIO bit is set, then the DIO line functions as an independent high voltage digital input output pin.

  Setting bit DCTL:IEN in this mode, enables a signal level change interrupt, informing the microcontroller that a level change has occurred on the DIO line.

- JOIN mode: If the DCTL:DIO bit is cleared, then the DIO/CQ outputs function together to provide a single, double drive strength, IO-Link conformal output. The outputs, DIO/CQ, must be externally shorted together. When in this mode, the DCTL:HS and DCTL:LS no longer have any effect on the output state.

6.1 DIO mode output control

In DIO mode there are two alternatives for controlling the pin output state: via SPI (DCTL:EXT reset) or directly via pin CTLD (DCTL:EXT set). Tables 2 & 3 show how the output is controlled in both cases respectively.

Mode	DCTL:HS	DCTL:LS	DIO Channel output state
Off	0	0	HiZ
Low	0	1	0
High	1	0	1
Illegal	1	1	HiZ

Table 2 DIO control via SPI - DCTL:EXT='0'

If bit DCTL:EXT is set, bits DCTL:HS and DCTL:LS function as configuration bits, which configure the DIO output to be a PNP, NPN or Push-Pull driver.

			DIO Channel Output State	
Mode	DCTL:HS	DCTL:LS	CTLD='1'	CTLD='0'
Inactive	0	0	HiZ	HiZ
NPN	0	1	0	HiZ
PNP	1	0	1	HiZ
Push-Pull	1	1	1	0

Table 3 direct DIO control via pin CTLD - DCTL:EXT='1'

The high and low side switches are identical and have an on-state resistance of R_{SW}. Any inactive switch acts as a zener diode limiting the voltage on the DIO line to V_{ZEN} above VPLUS (high-side switch), or V_{ZEN} below GND (low-side switch). This allows rapid switch-off for inductive loads.

The DIO data level is monitored for signals, filtering out pulses with a duration of less than t_{ND}. The decision threshold for the DIO data level is determined by the CFG:RF bit. Where this is '0', the IO-link standard absolute levels are used, and where the bit is '1' the threshold is referred to VPLUS/2.

6.2 SIO mode control

In the SIOActive state, the high-side or low-side switches are switched according to the CCTL:HS and CCTL:LS bits. It is not legal to switch both on simultaneously, and this register setting will disable both switches. The high-side and low-side switches are identical, and have an on-state resistance of R_{SW}. Any inactive switch acts as a zener diode limiting the voltage on the CQ line to V_{ZEN} above VPLUS (high-side switch), or V_{ZEN} below GND (low-side switch). This allows rapid switch-off for inductive loads.

7 IO-Link UART peripheral

The HMT7748 contains an IO-Link UART peripheral for bidirectional communication according to the IO-Link Standard [1]. The peripheral is controlled, and data is exchanged, via SPI register accesses. In an application where pins CQ and DIO are coupled together i.e. JOIN mode, then a reference to CQ in the following refers to the shorted pair.

7.1 Multi-octet mode

7.1.1 SIO mode

Fig. 7 shows the IO-Link UART peripheral state machine. When the CCTL:SIO bit is set, the HMT7748 is set to Single Input Output mode. In this mode the HMT7748 has the following states:

- SIOActive: The CQ line is driven according to the setting of the CCTL:HS and CCTL:LS bits.

  The internal UART does not run in this state and so master messages are only detected if a wake-up request from the master is received, which switches the HMT7748 to the SIOListen state. If the output is set to high impedance (CCTL:HS=LS='0'), then the HMT7748 can not receive a wake-up request from the master. It is therefore necessary to switch to IO-Link mode (CCTL:SIO='0') if communication detection is required with a high impedance output.

- SIOListen: The HMT7748 has experienced a short-circuit via a wake-up request from the master.

  Both the high side and low side switches are off, and the restart timer is running. Transitions on the CQ line are read as data, and stored in the data buffers (FR0:DATA[7:0] to FR14:DATA[7:0]). If a complete, valid, master message is received, then the state changes to Transmit, an interrupt is generated and the restart timer is reset.

  If the timer expires, then the HMT7748 returns to the SIOActive state and the CQ line is driven again after the transmission.

7.1.2 IO-Link mode

At start-up, and if the CCTL:SIO bit is cleared by the user, the HMT7748 enters IO-Link mode. In this mode the HMT7748 has the following states:

- IOListen: Transitions on the CQ line are read as data, and stored in the data buffers. Once a complete master message has been read, or an error is experienced in reception (eg. bad parity, checksum or time-out), then the state changes to Transmit.

7.1.3 Transmit mode

Following reception of an IO-Link master message the HMT7748 enters the following state:

- Transmit: The HMT7748 is waiting on data from the microcontroller, or is in the process of transmitting data on the CQ channel. The HMT7748 will revert to IOListen or SIOActive on completion of the transmission, or if an abort is generated by the microcontroller by writing a LINK:END command.

  If the HMT7748 has entered Transmit from an SIO mode, the microcontroller would normally now set the HMT7748 to IO-Link mode, such that the HMT7748 continues to listen for further information from the master.

If the HMT7748 experiences a short-circuit during Transmit, then the STATUS:SSC bit is set, and the HMT7748 returns to either IOListen or SIOListen.

7.1.4 IO-Link UART peripheral (Multi-octet mode) state machine

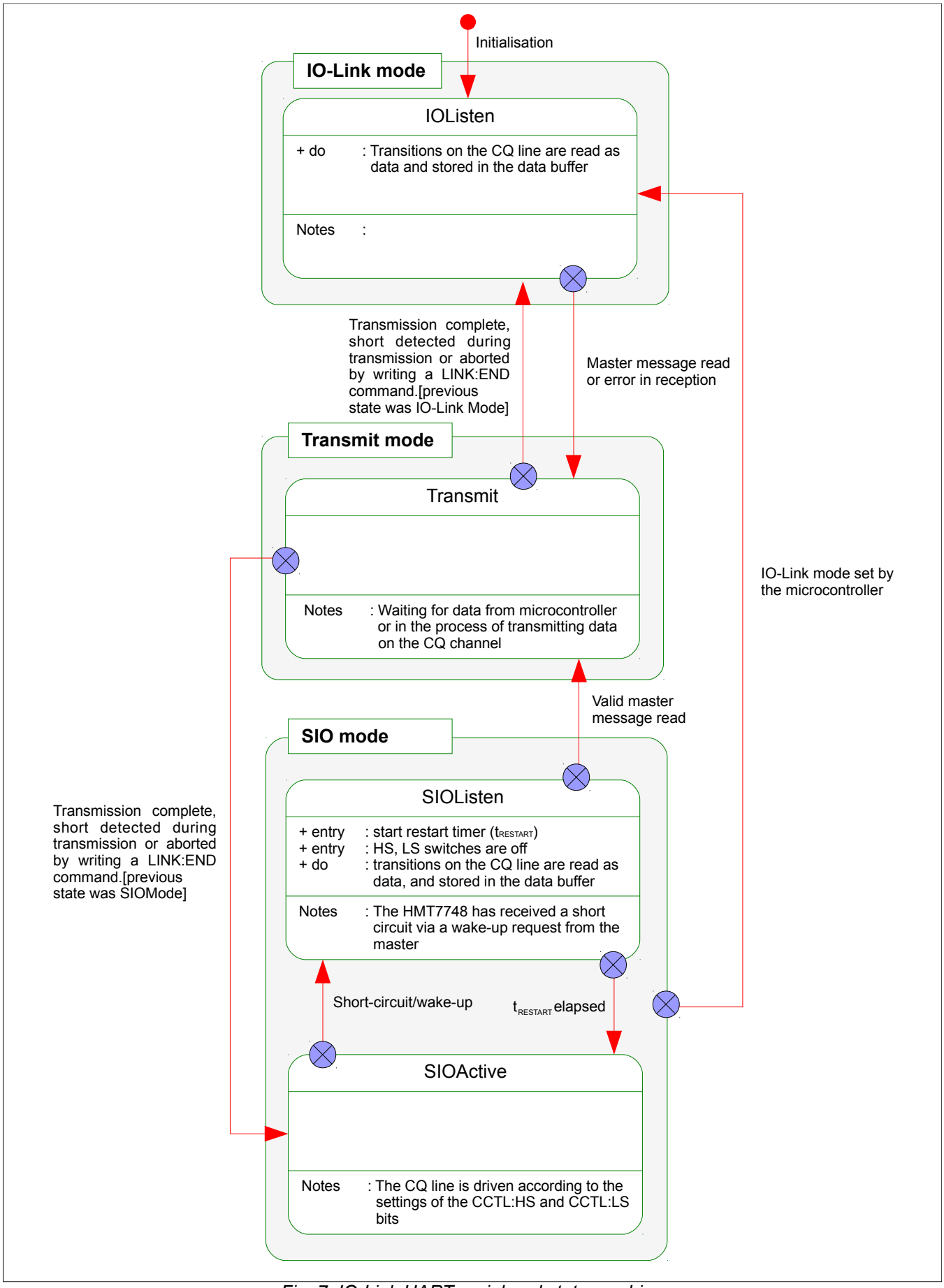


Fig. 7: IO-Link UART peripheral state machine

7.1.5 Interrupt handling

The HMT7748 signals an event to the microcontroller using the INT pin, which is intended to be configured as a level sensitive interrupt.

7.1.6 Data interrupt handling

If the STATUS:DAT bit is read as active (high) on an SPI access, then the HMT7748 is halted in a WAIT condition and is waiting for either a LINK:END or LINK:SND command from the microcontroller. While the HMT7748 is in the WAIT condition the interrupt pin (INT), the STATUS:INT bit and the STATUS:DAT bit remain active continuously. Data can be read and written to the HMT7748 registers while in the WAIT condition. Typically the LINK register and FR registers are accessed to read the incoming data, and the FR registers are written to set up the outgoing data. As the HMT7748 is halted, it will not generate further data interrupts in the WAIT condition.

When the microcontroller sends either a LINK:END or LINK:SND command, the interrupt pin (INT), the STATUS:INT bit and the data bit, STATUS:DAT, are cleared within 220ns of the last SCK edge of the SPI write access. If the microcontroller detects an active interrupt after the SPI access, or if the STATUS:DAT bit is read as active (high) on a subsequent SPI access, then new data is available.

7.1.7 Short circuit, over-temperature and under-voltage interrupt handling

The INT pin and the STATUS:INT bit are additionally active (high) if the last value of the short-circuit, under-voltage or over-temperature status bits communicated on the SPI are different to the current value. The HMT7748 handles short-circuit and over-temperature autonomously and does not require a reaction from the microcontroller. It is possible for these status bits to change at any time, and so the interrupt may be removed between entering the interrupt service routine and reading the status on the SPI. The interrupt will be removed during the next SPI access to the HMT7748. If an SPI access is made without checking the value of these bits, as is typical during processing of a data interrupt, it is normal to record the status values from the final access, or to explicitly add an extra SPI access.

7.1.8 Interrupt handler structure

The interrupt handler will typically have the following sequence:

```
read the HMT7748 status with a read access from the LINK register
if (STATUS:DAT is active)
   {
   analyse the STATUS:CHK bit, read the FR registers and write an appropriate response into the FR registers
   send a LINK:SND or LINK:END command as appropriate
   };
update the microcontrollers copy of the short-circuit, under-voltage and over-temperature status based on the
status bits received in the previous access. Take action if necessary.
```

7.1.9 Changing to and from SIO mode

The HMT7748 should be placed into IO-Link mode as soon as communication with the master is established.

Typically a switch from SIO mode (CCTL:SIO='1') to IO-Link mode (CCTL:SIO='0') is made during the WAIT condition when a valid message is detected from the master. A switch from IO-Link mode to SIO mode is typically made shortly after the device response to the FALLBACK command from the master has been sent. The switches themselves are, however, only activated by the microcontroller after the period defined in the IO-Link specification [1].

The HMT7748 may be switched from SIO mode to IO-Link mode at any time without disturbing data reception or transmission. A switch from IO-Link mode to SIO mode may disturb data reception if a master is in the process of transmitting, and the UART is therefore reset if this occurs.

7.1.10 SPI register writes outside interrupt service routines

The interrupt service routine will typically access the SPI, and so it is necessary to avoid a collision between an interrupt service routine SPI access and any other SPI access made from the microcontroller. Accessing the SPI will clear a short circuit or over-temperature interrupt, and so the received value of these bits must be recorded by the microcontroller. If a function makes a number of sequential SPI accesses, then it is reasonable to ignore these status bits on all but the last access, and record the values read on this last access.

It is not necessary to check the STATUS:DAT bit outside the interrupt service routine, since the data interrupt remains active until the microcontroller responds.

7.2 Single octet UART mode

The HMT7748 supports an operating mode called Single octet UART mode, which performs a simplified data transfer function, transferring one octet at a time in either direction. In this mode, M-sequence type recognition (MSEQ:M2CNT), the number of on-demand data octets (MSEQ:OD1, MSEQ:OD2) and checksum verification/generation are disabled and, therefore, must be realised by the microcontroller.

Note, that an exchange is always triggered by the master. It is not possible to transmit data without first receiving valid data.

Fig. 8 shows the single octet UART mode state machine. When the CCTL:SGL bit is set by the microcontroller, the HMT7748 is set to single octet UART mode.

7.2.1 Buffering

The FR0 register and the HMT7748 UART internal register together provide double buffering of data in receive and single buffering in transmit. in order to avoid buffer over- or under-runs it is necessary for the microcontroller to:

- read FR0 before the UART writes a new octet in Receive mode (delay ca. $11xT_{BIT}$), or
- write FR0 before the UART requires a new octet in Transmit mode (delay ca. $3xT_{BIT}$).

7.2.2 Receive mode

In Receive mode the HMT7748 has the following states:

- Receive wait: The HMT7748 has received a complete master octet via the CQ channel. A data interrupt is generated (STATUS:DAT='1') and the received octet is placed in the FR0 register.

  The microcontroller has access to the FR0 register and reads the received octet.

  The HMT7748 is now waiting for a response from the microcontroller, which either writes LINK:END to continue receiving, or FR0 to initiate sending. (A LINK:END should **not** be sent after receiving the last octet.)

  The UART continues to run in this state receiving the following frame. A buffer over-run will result if the microcontroller does not provide a response before the frame completes. A UART frame is 11 bits, which at 230.4kBaud gives a period of 47µs for the two SPI accesses, each of 16 bits. At 4MHz SPI this corresponds to an SPI delay of 8µs.

  Once the expected number of octets is received, the microcontroller initiates sending by writing the first octet in the response M-sequence to FR0, thereby switching the HMT7748 to Transmit mode (see §7.2.3). (In single octet UART mode the equivalent of a LINK:SND command is achieved by writing to FR0).

  Error conditions: parity error, stop bit, time-out (more than $4xT_{BIT}$ waiting for the next UART frame on the CQ line), or buffer under-run are signalled with a data interrupt (STATUS:DAT='1') with additionally STATUS:CHK='1'. The microcontroller should respond by writing LINK:END and discarding any received octets.

  The master stops sending after the last master octet and so a time-out will generally be detected by the HMT7748 in the delay while the microcontroller is preparing the response. The condition is held internally in the HMT7748 and discarded by the HMT7748 when FR0 is written by the microcontroller, initiating transmission. The time-out is therefore not reported to the microcontroller in this case.

- Receive interim: The UART receives data on the CQ line and copies this to the FR0 register, switching to Receive wait on completion.

In SIOListen mode a received UART frame is only reported if the parity and stop bits are correct. The microcontroller must switch from SIO mode to IO-Link mode after reception of a valid UART frame before responding with LINK:END, otherwise the HMT7748 returns to SIO mode conflicting with the further master transmission.

7.2.3 Transmit mode

Transmit mode is entered when the microcontroller writes FR0 while the HMT7748 is in the Receive wait state. The UART reads this value from the FR0 register, emptying the buffer, and starts transmitting. The HMT7748 enters the Transmit wait state.

The HMT7748 provides a single octet data buffer and requests further data whenever this buffer is empty, including during the transmission of the previous octet. It is only necessary to ensure that this buffer is refilled before the UART needs to send the next octet.

The maximum allowed time between the starts of two subsequent frames on IO-Link is 11 T_{BIT} frame + 3 T_{BIT} pause = 14 T_{BIT}, which at 230.4kBaud gives a period of 60µs for the 16 bit SPI access. At 4MHz SPI this corresponds to an SPI delay of 4µs.

In Transmit mode the HMT7748 has the following states:

- Transmit wait: The HMT7748 requests a new octet by sending a data interrupt (STATUS:DAT='1').

  The HMT7748 is waiting for a response from the microcontroller, which either writes FR0 with a new octet to continue transmission, or LINK:END to terminate transmission.
- Transmitting (buffer empty) The UART sends the current octet.

  A further response is requested from the micro-controller, by sending a data interrupt (STATUS:DAT='1'). If the micro-controller provides a further octet, this is placed in the buffer and the state changes to Transmitting (buffer full), if the micro-controller writes LINK:END, then the state changes to Transmitting (terminating).

  If the microcontroller does not provide an octet before the UART transmission completes, then the state changes to Transmit wait.
- Transmitting (buffer full) The UART sends the current octet. On completion, it sources the next octet from the buffer, and the state changes to Transmitting (buffer empty).
- Transmitting (terminating) The UART sends the current octet. On completion, the PHY returns to idle.

7.2.4 Timing errors in transmit

The microcontroller can cause a timing error in Transmit mode if the delay in response is too long. These errors are not monitored by the HMT7748. A minimum inter-frame time delay of $1xT_{BIT}$ is, however, guaranteed by the HMT7748.

7.2.5 Error conditions in transmit

Error conditions are reported to the microcontroller as either short-circuit (STATUS:SSC='1', reported following a delay of t_{RETRY}), over-temperature (STATUS:SOT='1'). The conditions are handled autonomously by the HMT7748 and no intervention by the microcontroller is necessary. The normal data flow is preserved and the HMT7748 will request further octets from the microcontroller as if the error were not present. These octets are silently dropped and no attempt is made to transmit them. Under error conditions, then transmission *may* be terminated by the microcontroller using LINK:END='1'.

7.2.6 *Single octet UART mode state machine*

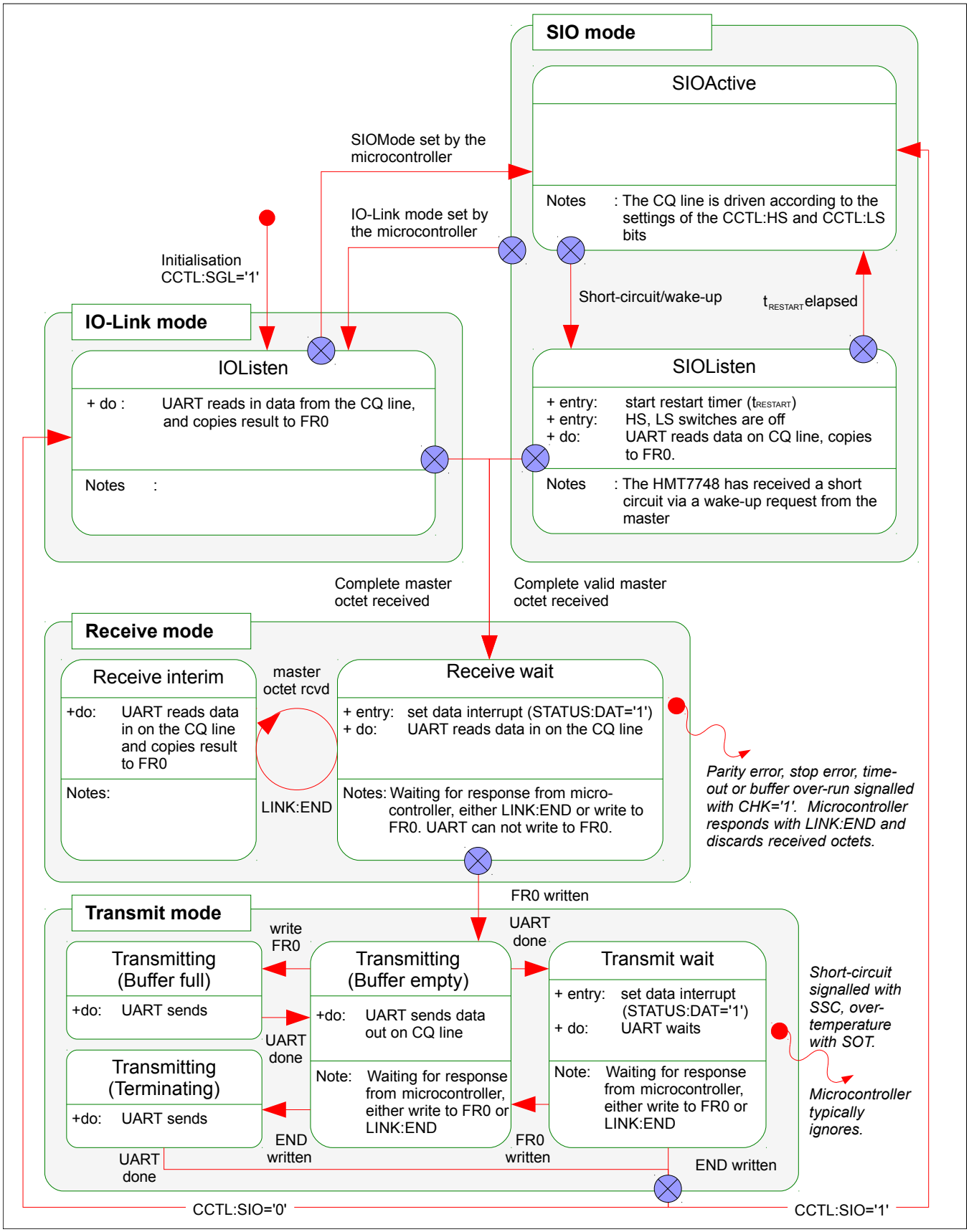


Fig. 8: Single octet UART mode state diagram

7.2.7 Synchronisation in single octet UART mode

The HMT7748 uses a PLL (phase-locked loop) to continuously lock the UART receive and transmit frequency to the master frequency. A few octet values (00_h, 80_h, $e0_h$, $f8_h$ and fe_h) do not provide information which can be used to correct the PLL frequency, and a continuous sequence of these values could prevent the PLL performing frequency tracking for some time. In IO-Link operation, however, it is not possible to create such M-sequences as the defined format of the M-sequence, and in particular the checksum, guards against this.

A continuous sequence of these octets is possible when the single octet UART mode is used in a proprietary mode, eg. for code download. In this case, the insertion of a synchronisation octet (aa_h) at least every 75ms is required, taking into account a worst case dissipation change (1W) in combination with a worst case oscillator temperature drift. The interval of 75ms is equivalent to 240 octets at 38.4kBaud assuming an inter-frame delay of 1 bit. We recommend the insertion of a synchronisation octet every 32 octets.

7.3 Transparent mode

The HMT7748 supports an operating mode for transparent communication of UART frames. In this mode, the frames are received and transmitted from a UART peripheral in the microcontroller, and the function of the DUAL PHY device is reduced to that of a physical level converter. This mode is supported by dual use of the MOSI and MISO pins, maintaining the low overall pin-count and a restricted use of microcontroller resources.

Transparent mode is entered by setting the CCTL:TRNS register bit to '1' via the SPI. In this mode the IO-Link state machine in the HMT7748 and the PLL are placed in reset. The interrupt line and status monitoring for reset, short-circuit, over-temperature and under-voltage events continue to function.

7.3.1 Pin functions in transparent mode

In transparent mode, the MOSI and MISO pins are used for both SPI communication, and for the transparent path. The SS pin controls the use of the MOSI and MISO pins, according to Table 4.

	SPI comm's	transparent path	MOSI	MISO
SS='0'	SPI comm's active	CQ output switch control frozen	SPI data in	SPI data out
SS='1'	SPI comm's frozen	transparent path active	CQ output switch control	filtered CQ line level

Table 4 Pin dual use in transparent mode

An SPI communication in transparent mode is shown in Fig. 9. Initially the HMT7748 is driving the CQ line, an SPI exchange is then conducted in which the HMT7748 is instructed to stop driving the line, and finally the IO-Link master drives the CQ line.

Typically the microcontroller SPI access routine will record the MOSI level in use before setting SS='0' to start an SPI access, and assert this value again on the MOSI line before setting SS='1'. The microcontroller should preset the MOSI pin to the required level before the first SPI access enabling transparent mode. Support for this may however be automatic depending on the microcontroller.

The SPI connection to the HMT7748 is not suitable for a bus connection of multiple SPI slaves in transparent mode as the MOSI line is permanently driven.

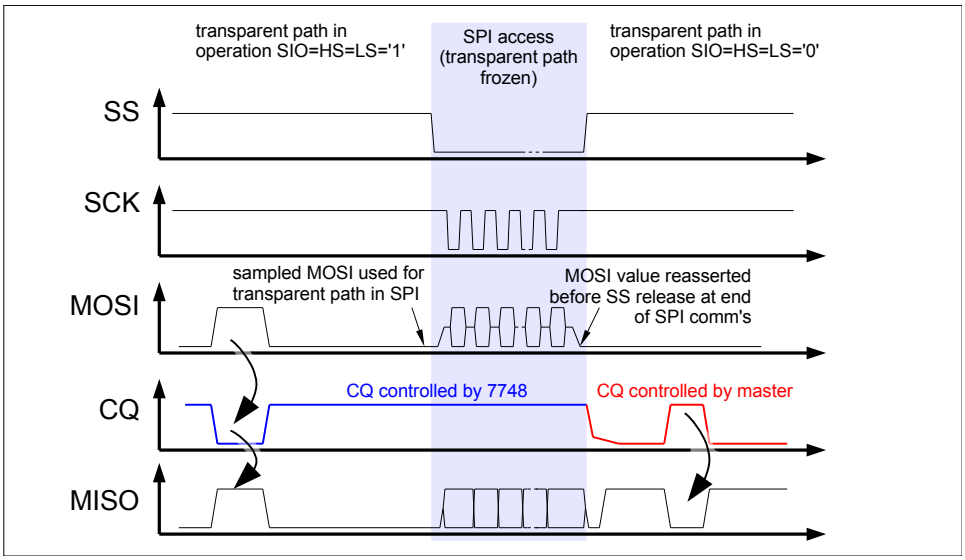


Fig. 9: Illustration of operation in transparent mode

7.4 Transparent mode output path

With SS='1', the level of the MOSI pin controls the output switches according to the SIO, HS and LS bit settings as shown in Table 5. Where SS='0' for SPI access the level latched on the MOSI line is frozen, and used in the place of the MOSI line itself.

The CCTL:HS and CCTL:LS bits function as enables for the high-side and low-side switches respectively, and select operation as a high-side, low-side or push-pull device. Note that the logical path from MOSI to CQ is inverting.

CCTL:SIO	CCTL:HS	CCTL:LS	operation	short-circuit
1	0	0	SIOListen operation	short reported after retry
1	0	1	SIO low-side operation	
1	1	0	SIO high-side operation	
1	1	1	SIO push-pull operation	
0	0	0	IOListen operation	short timers reset
0	0	1	do not use	
0	1	0	do not use	
0	1	1	push-pull IO-Link operation	short reported immediately

Table 5 Transparent mode operation

In transparent SIO operation (CCTL:TRNS='1', CCTL:SIO='1') a short is only reported after N retries, see t_{RETRY}, which is suitable to indicate the presence of a valid IO-Link wake-up pulse. In transparent IO-Link operation (CCTL:TRNS='1', CCTL:SIO='0'), a short is reported immediately after t_{SHORT}. In both cases the device will attempt to drive the line again after t_{RETRY} and then $t_{RESTART}$ without intervention from the microcontroller. The output switches are disabled while a short is reported, protecting the device from excessive dissipation.

The short condition and associated internal timers can be reset by setting the IOListen operation (CCTL:TRNS='1', CCTL:SIO=CCTL:HS=CCTL:LS='0'), which allows switching to push-pull IO-Link operation after valid data has been received. Following a cleared short condition, a new driving operation should only be selected after receiving valid IO-Link data or waiting for at least $t_{RESTART}$.

7.4.1 Transparent mode input path

With SS='1' in transparent mode, the level of the MISO line is the inverted level of the CQ signal. The signal is filtered with a constant delay filter, t_{ND}, to remove line glitches.

7.4.2 Leaving transparent mode

Transparent mode is left by clearing the CCTL:TRNS register bit to '0' via the SPI.

8 IO-Link physical layer

8.1 UART frame

bit #	1	2	3	4	5	6	7	8	9	10	11
significance	START	LSB							MSB	PARITY	STOP
level	0	b0	b1	b2	b3	b4	b5	b6	b7	p	1

Table 6: UART Frame definition

A logic '1' is transmitted as a low level on the CQ line, and a logic '0' is transmitted as a high level on the line. The idle state for the CQ line is low.

Even parity is used, that is, there will always be an even number of logical '1' bits in the 9 bit concatenation of the data bits b[7:0] and the parity bit.

8.2 M-sequence interpretation

The data direction is derived from the MSB of the first octet of the master message, “M-sequence control” (MC), where a '1' denotes a read operation and a '0' a write. see [1] for further details.

MSB							LSB
R/W	Comm chan.	Address					

Table 7: M-sequence control (MC) octet

The M-sequence type is derived from bits [7:6] of the second octet of the master message, “Checksum/M-sequence type” (CKT), which have permissible values of 2'b00, 2'b01, or 2'b10, and denotes whether the structure of the message is of Type 0, Type 1 or Type 2. See [1] for further details.

MSB							LSB
M-seq. type	Checksum						

Table 8: Checksum/M-sequence type (CKT) octet

The total length of the received M-sequence is determined according to Table 9, and is dependent on the M-sequence' type and on the transfer direction (READ or WRITE).

	CKT:M-seq.type [7:6]	Received M-Sequence length	
		READ, MC:R/W = '1'	**WRITE**, MC:R/W = '0'
Type 0	00	2 octets	3 octets
Type 1	01	2 octets	2 octets + f(OD1)*
Type 2	10	M2CNT	M2CNT+f(OD2)

Table 9: Receive M-sequence lengths

f(*OD1), f(OD2)* and *M2CNT* are used to configure the HMT7748 for M-Sequence reception and are configured through register MSEQ as follows:

- *f(OD1), f(OD2):* defines the received number of on-demand octets, where support is only provided for data widths of 1, 2 and 8 octets and not 32. The values are determined from MSEQ:OD1[1:0] for type 1 sequences and MSEQ:OD2[1:0] for type 2 sequences according to Table 10.

MSEQ:OD1[1:0]	*f(OD1)* (On-demand data)
00	*illegal**
01	2 octets
10	8 octets

MSEQ:OD2[1:0]	*f(OD2)* (On-demand data)
00	1 octet
01	2 octets
10	8 octets

Table 10: Permissible values of MSEQ:OD1 and MSEQ:OD2

- *M2CNT:* defines the expected octet count on a read operation. Its value corresponds to the value of field MSEQ:M2CNT[3:0]

The total data buffer size is 15 octets. If an M-sequence of a length greater than this is required for reception or transmission, then the single octet UART mode should be used (see section 7.2).

* A setting of MSEQ:OD1[1:0]=00 is used for backwards compatibility. In this case M2CNT + f(OD2) defines the length of received type 1 M-sequences.

8.2.1 Example settings

Table 11 shows examples to illustrate the correct register settings for M2CNT, OD1 and OD2 for different combinations of PREOPERATE and OPERATE M-sequences.

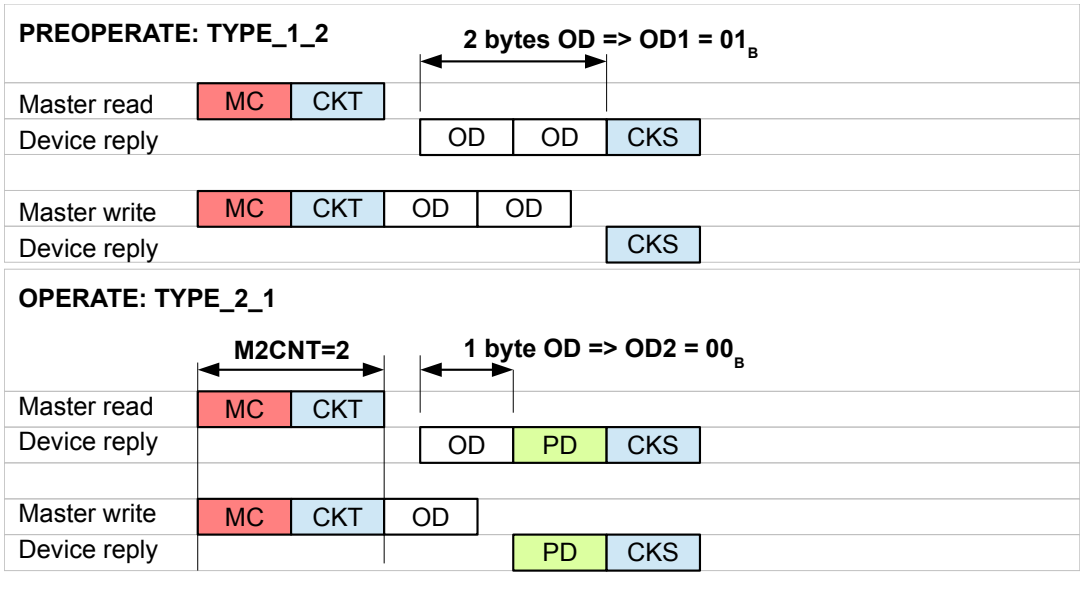
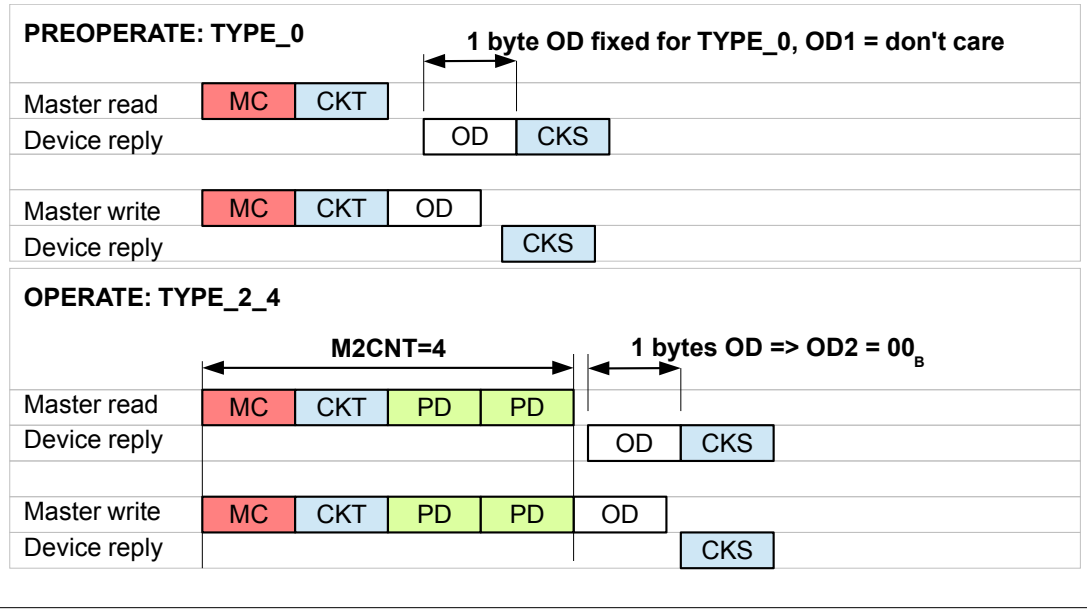
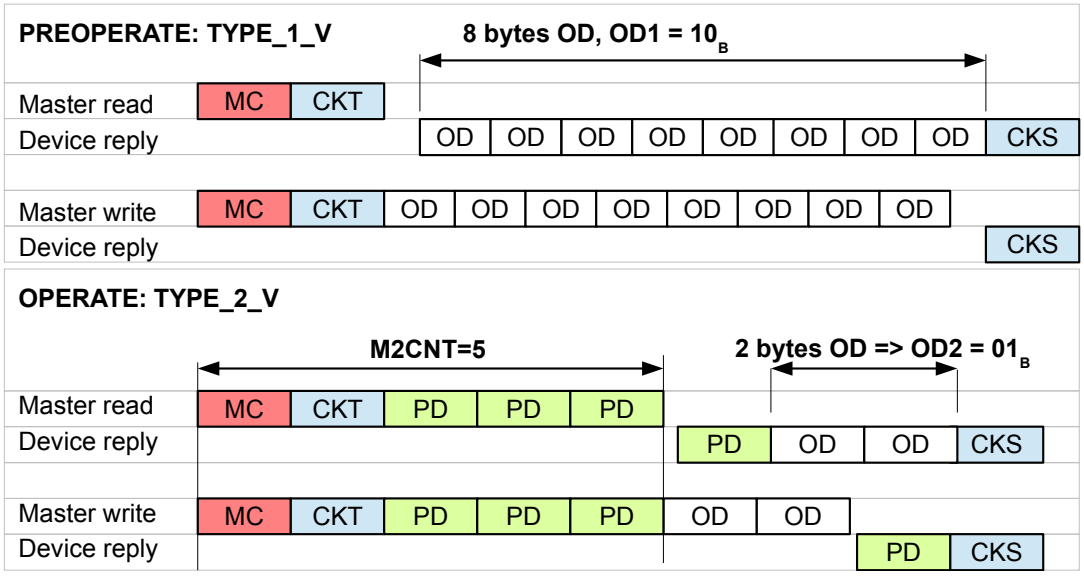
Nr.	Type
1	
2	
3	

Table 11 Example M2CNT, OD1 and OD2 register settings

8.3 Checksum calculation and verification

The checksum for an out-going message is calculated by the HMT7748, by logically exclusively OR'ing all LINK:CNT octets of the message, with a starting value of 0x52h. For this calculation the written value of the checksum register should be zero. The checksum is compacted from 8 bits to 6 bits using the algorithm of Table 12:

Bit	Calculation
C[5]	D[7] xor D[5] xor D[3] xor D[1]
C[4]	D[6] xor D[4] xor D[2] xor D[0]
C[3]	D[7] xor D[6]
C[2]	D[5] xor D[4]
C[1]	D[3] xor D[2]
C[0]	D[1] xor D[0]

Table 12: Checksum compaction

The HMT7748 then inserts this 6-bit checksum into the lower bits of the last octet sent (“Checksum/status octet”).

MSB							LSB
Event flag	PD Invalid	Checksum					

Table 13: Checksum/status (CKS) octet

The HMT7748 calculates the expected checksum for an incoming message, by exclusively OR'ing the octets of the master message, with a starting value of 0x52h. For this calculation the Checksum/M-sequence type (CKT) octet is used, but with all of the bits of the Checksum field set to zero. The calculated and expected checksum are compared and the STATUS:CHK bit is set accordingly.

8.4 Data signal receive

The baud rate for signal reception is set by the CFG:BD bit. Both 38.4kBaud and 230.4kBaud are supported.

The CQ data level is monitored for signals, filtering out pulses with a duration of less than t_{ND}. The decision threshold for the CQ data level is determined by the CFG:RF bit. Where this is '0', the IO-Link standard absolute levels are used, and where the bit is '1' the threshold is referred to VPLUS/2.

The first transition is the start reference of the frame. After this, data is sampled at the centre of each bit time. Bits are read into the data buffers, removing the start and stop bits. The fill level is recorded in the LINK:CNT field.

Once the expected number of UART frames have been read, the checksum and parity bits for the message are checked, and the STATUS:CHK bit set appropriately. The STATUS:DAT bit is set, and an interrupt is generated.

Consecutive UART frames are expected from the master within a period of $3xT_{BIT}$. If a time of $4xT_{BIT}$ is exceeded, then both the STATUS:DAT and STATUS:CHK bits are set and an interrupt is generated on the INT pin.

The HMT7748 will then enter the Transmit state and wait for the microcontroller to read the data and prepare a return message, signalling completion by writing a '1' to either the LINK:SND or LINK:END register bits.

8.5 Data output

The baud rate for transmission is set by the CFG:BD bit. Both 38.4kBaud and 230.4kBaud are supported.

The number of message octets for transmission are written into the LINK:CNT field and sent following writing bit LINK:SND. The START, STOP and PARITY bits are appended to create the UART frames, and the checksum calculated and stuffed in the message. The data is sent by using push-pull operation of the output switches.

Writing either the LINK:SND or LINK:END bit clears the STATUS:DAT and STATUS:CHK status flags.

The data output is synchronised using the HMT7748's internal PLL clock.

As defined in the IO-Link specification [1], the device has a maximum of $10xT_{BIT}$ periods to process the incoming message and prepare the response. A delay of up to $T_{BIT}/16$ can be incurred in the HMT7748 due to synchronisation with the internal PLL clock, leaving the microcontroller slightly less than $10xT_{BIT}$ to respond.

8.6 Clock recovery

The HMT7748 has an internal RC clock with a nominal frequency of f_{CK}.

The filtered data line is monitored for transitions while in the IOListen and SIOListen states. When a first rising edge is seen, the internal PLL clock phase is aligned to the incoming data. The PLL clock corrects its operational frequency on the detection of further rising edges. See §7.2.7 regarding detailed operation in single octet mode.

The clock correction has a resolution of f_{RES} and a stability of f_{STAB} over the duration of a message.

9 Short circuit detection

In the case of a short circuit or a wake-up request from the master, the CQ, or DIO, channel current will exceed the set short-circuit threshold. When this occurs continuously for a period longer than t_{SHORT}, the output transistors for the affected output are switched off.

In IO-Link mode, the event is signalled immediately to the microcontroller via the STATUS:SSC bit and an interrupt is generated.

With CQ in SIO mode or with DIO in independent mode, a number of retries, N_{RETRY}, are attempted with a delay of t_{RETRY}. If these are unsuccessful then the event is signalled to the microcontroller via the STATUS:SSC bit and an interrupt is generated. A restart timer is started, with period $t_{RESTART}$. If this timer elapses without intervention by the microcontroller or without reception of a valid IO-Link message, then the HMT7748 will attempt to drive the line again. In the event of a continued short-circuit, this cycle will repeat indefinitely.

The short-circuit current thresholds are set by CCTL:SCT[2:0] and DCTL:SCT[2:0]. Where JOIN mode is requested, the DCTL:SCT[2:0], DCTL:HS and DCTL:LS bits no longer have any effect on the output state or short circuit detection.

CCTL:SCT, DCTL:SCT	Threshold DIO/SIO	Threshold JOIN mode	CCTL:SCT, DCTL:SCT	Threshold DIO/SIO	Threshold JOIN mode
decimal	(mA)	(mA)	decimal	(mA)	(mA)
4	110	220	0	190	380
5	130	260	1	210	420
6	150	300	2	230	460
7	170	340	3	250	500

Table 14: Short-circuit threshold current, I_{SET}, CQ and DIO

10 Maximum current output

The switches have an independent saturation current of I_{SAT}, and will not draw more current than this. If, however, the CQ and DIO pins are configured to create a single output (JOIN mode), then the saturation current in this case will be $2xI_{SAT.}$ The power supply must be able to supply this current for the duration T_{SHORT} to prevent a supply voltage drop on VPLUS.

11 Under-voltage detection

If the voltage on the VPLUS is below the V_{UV} threshold, then the status bit UV is set. An interrupt is generated if this status is different to the status reported in the last SPI exchange.

The under-voltage threshold is set by CFG:UVT[2:0].

CFG:UVT	Threshold	CFG:UVT	Threshold
decimal	(V)	decimal	(V)
0	17.0	4	11.5
1	15.5	5	9.5
2	14.0	6	8.0
3	13.0	7	6.5

Table 15: Under-voltage thresholds

12 Short term power loss

If the supply on the VPLUS fails then reverse current from V3V3 to VPLUS and from V5V to VPLUS is blocked. A residual leakage current of $I_{PLUSREV}$ may still flow in this time. Appropriate dimensioning of the capacitors C_{V3V3} and C_{V5V} can be used to maintain the power supply during this event.

13 Temperature measurement

The measured temperature in celsius can be read from the HMT7748 from the TEMP:TEMP[6:0] register. The temperature is given as shown in Fig. 10.

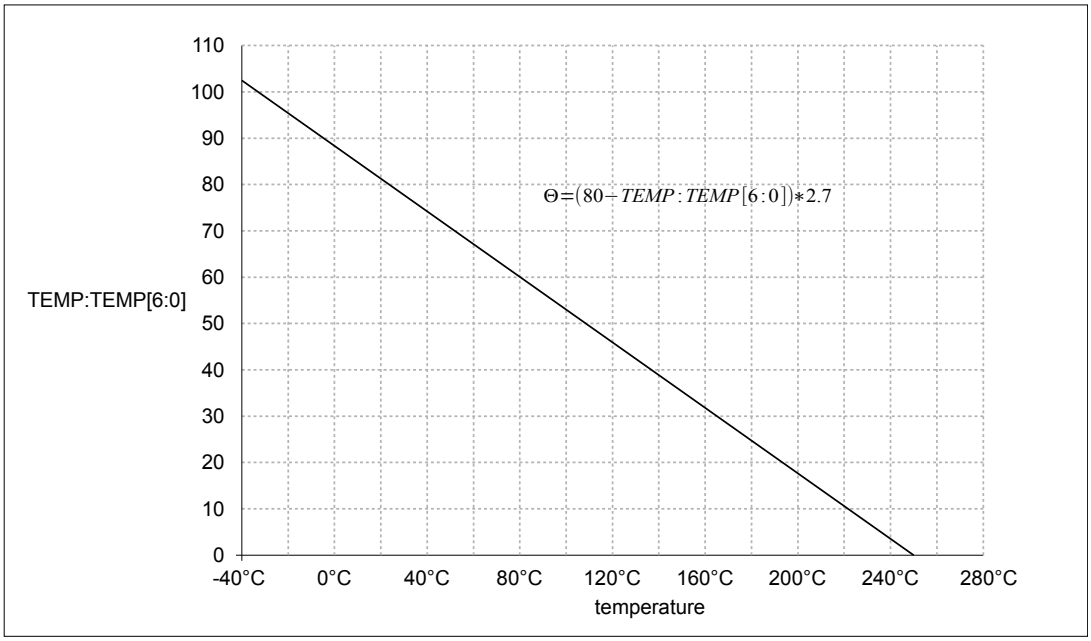


Fig. 10 HMT7748 temperature measurement

14 Thermal shutdown

The STATUS:SOT status bit is a filtered version of the output of the temperature sensor. When the HMT7748 temperature exceeds the threshold this bit is set to '1', when the temperature is below the threshold the bit is set to '0'. The trip threshold is determined by the set-point in register THERM:TH[4:0] as shown in Fig. 11

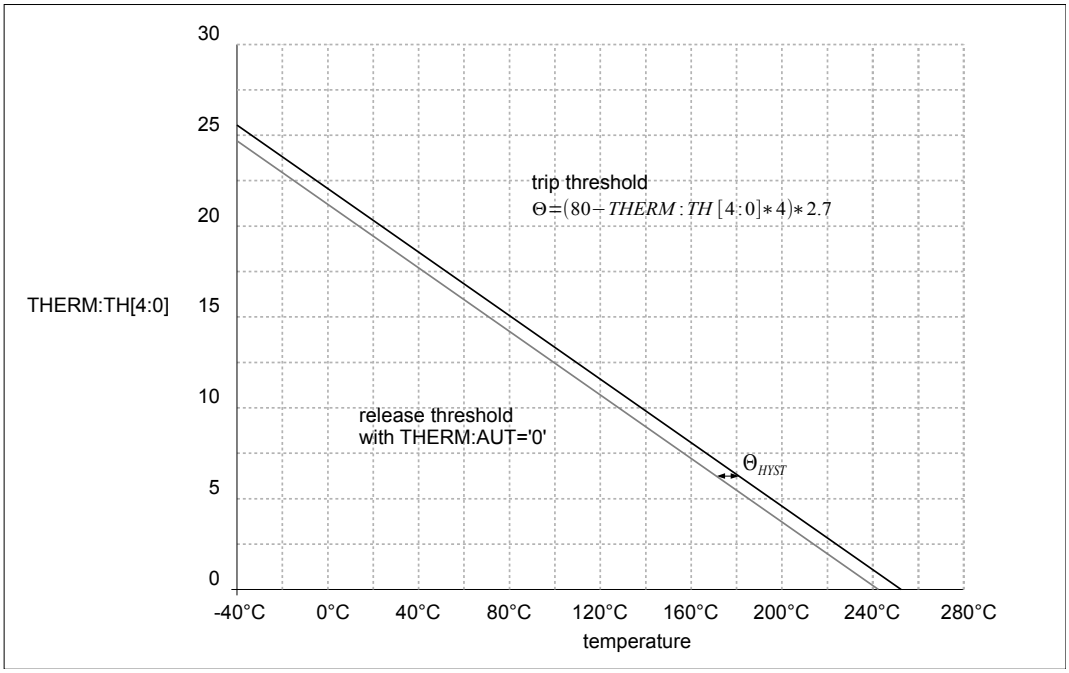


Fig. 11 HMT7748 thermal shutdown configuration

If the trip threshold is exceeded, the output switches are disabled, the event is signalled to the microcontroller via the status register (STATUS:SOT) and an interrupt is generated.

14.1 Automatic operation

If the THERM:AUT bit is '0' and a temperature in excess of the set point is reached, then the threshold is automatically moved to a release threshold Θ_{HYST} below the set point. When the temperature falls below this release threshold, the HMT7748 will return to a normal operating state and return the threshold to the original level.

15 LED outputs

Two current controlled outputs are provided to generate a LED current up to 8mA. The nominal LED current is defined by the settings of the LED:LED1 and LED:LED2 fields.

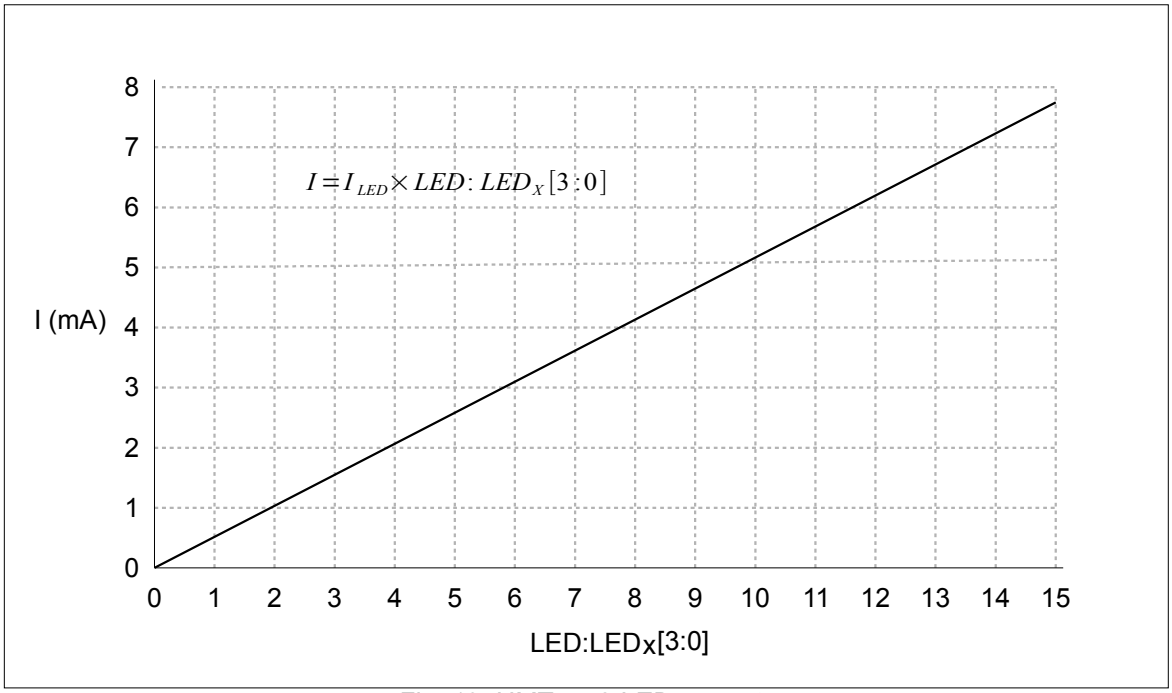


Fig. 12: HMT7748 LED currents

16 DC-DC converter

16.1 Converter configuration

The HMT7748 includes a DC-DC buck converter, which operates at a frequency configured by register DCDC:FSET[2:0], shown in Table 16. Irregular frequency steps have been carefully chosen so to avoid simple fractional multiples, such that it is possible to choose a controller frequency which does not interfere with a given sensor frequency.

DCDC:FSET	frequency (kHz)	DCDC:FSET	frequency (kHz)
4	500	0	1000
5	625	1	1250
6	710	2	1670
7	830	3	2000

Table 16 DCDC converter nominal operating frequency, F_{SET}

The output voltage, VDCDC, is configured by DCDC:VSET[2:0], shown in Table 17. Note that where operation of the 5.0V linear regulator is required, the VDCDC output voltage must be configured to be at least $V_{DCDC\_5V\_MIN}$.

DCDC:VSET	target output (V)	DCDC:VSET	target output (V)
0	5.0	4	7.8
1	5.6	† 5	8.6
2	6.1	6	9.6
3	6.8	7	10.5
† default value following reset.			

Table 17 DCDC output voltage, V_{SET}

Changes to the output voltage via VSET are executed in steps, with a delay of t_{VSET} for each step between $VSET_{MIN}$ and $VSET_{MAX}$. This minimises any over- or undershoot on VDCDC as the output voltage approaches the target value. This implies that a maximum delay of Δt_{VSET} can occur between this range.

If the DC-DC converter is not required, the pin DOUT is externally shorted to pin VDCDC.

16.2 DC-DC minimum supply voltage

In order to ensure stable operation of the DC-DC converter over the specified operating range and converter configuration, a minimum supply voltage must be applied on pin VPLUS. Fig. 13 provides a guideline for determining this voltage, based on the setting of DCDC:VSET and application load currents.

note: all measurements were performed at the nominal F_{SET} frequency of 1MHz, and with the following external components: C_{DCDC}=2.2µF, L_{DCDC} = 220µH.

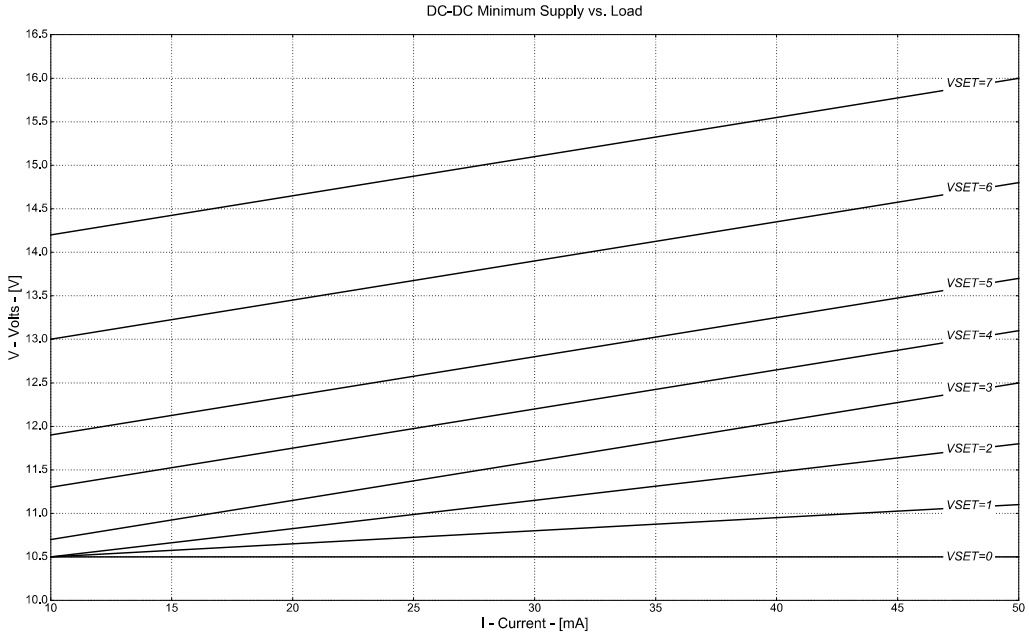


Fig. 13 Minimum VPLUS vs. Load for each VDCDC set voltage

16.3 Converter architecture

The buck converter consists of two internal MOS switches (PMOS and NMOS), an external capacitor, C_{DCDC}, and an inductor L_{DCDC}. The switches operate in anti-phase and, assuming no resistive losses, the output voltage (VDCDC) is equal to the duty ratio of the high side switch multiplied by the input voltage (VPLUS).

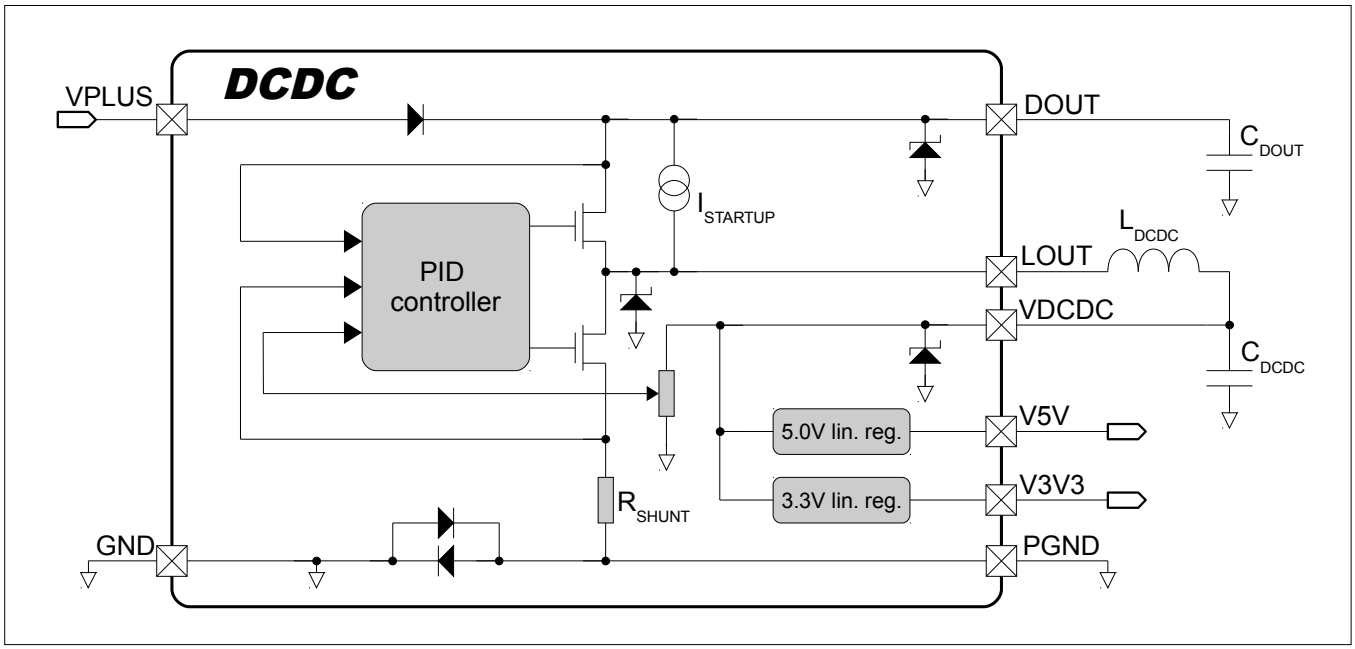


Fig. 14: DCDC converter block diagram

This block also includes a sense resistor to measure the inductor current, R_{SHUNT}, a series diode to prevent conduction during reverse polarisation and protection diodes to conduct residual inductor currents whenever switching ceases.

The high side switch is activated at the start of each cycle, and remains on for a length of time determined by the PID controller. This time is further limited by the time T_{LIMIT} which is determined by the input voltage and restricts the coil current increase in any one cycle. If the coil current exceeds the current threshold I_{LIMIT} at the start of the cycle, then activation of the high-side is completely suppressed.

The block monitors the voltage VDCDC and the input voltage DOUT.

16.4 Converter operation

16.4.1 Start-up

The converter will operate only when the following *operating conditions* are met:

- $V(V3V3)>V_{POR}$
- $V(V3V3)>V_{DCMIN}$
- bandgap stable
- oscillator toggling

Operation outside these conditions is prevented to protect the IC and the surrounding circuit.

Initially the converter is in a STARTUP state. In this state an internal current source attempts to source a current $I_{STARTUP}$ from pin DOUT to pin LOUT. Where LOUT is connected to VDCDC by an inductor, VDCDC is pulled up by this current. VDCDC rises until it reaches voltage $V_{STARTUP}$, where the source current is then regulated to maintain voltage VDCDC voltage at $V_{STARTUP}$. The converter remains in the STARTUP state until the operating conditions are met.

Bias is provided either by an HV bias circuit where the IC is in reset $V(V3V3)<V_{POR}$, or by a LV bias circuit once V3V3 is available. During the overlap period, the bias currents are doubled.

16.4.2 Entry to operation

Once the operating conditions are met, or when the DCDC:DIS bit is reset, then the converter passes through an ARM state for a duration of $T_{DCSTART}$ before starting operation. The switch controls are powered in this state, but set to off.

16.4.3 Leaving operation

If the operating conditions are no longer met, then the converter will pass back through the ARM state to the STARTUP state. If, however, the DCDC:DIS bit is set, then the converter will pass back through the ARM state to the SLEEP state. On leaving this operation, any residual energy in the coil is conducted to VDCDC via the protection diode between LOUT and PGND.

16.4.4 SLEEP state

The SLEEP state is reached after time $T_{DCSLEEP}$ by setting the DCDC:DIS bit via the microcontroller. In the SLEEP state no current is drawn on VPLUS or V3V3, and the switch control blocks are depowered. The SLEEP state is left by clearing the DCDC:DIS bit, or during a HMT7748 reset, that is, when V(V3V3)<V_{POR}.

16.4.5 BYPASS state

The BYPASS state is equivalent to the STARTUP state, and is reached after time T_{BYP_EN} by setting the DCDC:BYP bit via the microcontroller. In this mode, the $I_{STARTUP}$ current source is permanently enabled and the voltage on V_{DCDC} is held at $V_{STARTUP}$. Power to the devices on the V3V3 or V5V pins is now provided via the inductor and linear regulators. Leaving the BYPASS state is achieved by clearing the DCDC:BYP bit, whereby normal operation of the DCDC converter will resume after time T_{BYP_DIS}.This operation mode can be used if a device is operated at times in a low current consumption state, or suppression of converter switching noise is required for a temporary period.

16.4.6 Configuration

The DCDC converter is configured to run by default. If the DCDC converter is not required, then pin DOUT should be externally connected to pin VDCDC to supply the regulator via the internal series diode. Pin LOUT should be unconnected, and the microcontroller should disable the DCDC converter via the DCDC:DIS bit at start-up. To prevent potentially dangerous inrush currents at start-up, both C_{DOUT} and C_{DCDC} should remain unpopulated.

17 Linear regulators

In addition to the DCDC regulator, the HMT7748 includes two 50mA linear regulators supplied from the VDCDC pin, which have internally set output levels at V_{V3V3} and $V_{V5V.}$ The 3.3V linear regulator acts as the master, and the 5.0V linear regulator as the slave. The start-up time of the 5.0V linear regulator is thus dependent on the 3.3V level, and on the size of the 3.3V line capacitance, $C_{V3V3.}$ The regulators' dynamic start-up behaviour under different conditions of load capacitance can be seen in Fig. 15. A typical load of 10mA, a supply voltage of 24V with a rise time of 2.4V/µs on pin VPLUS were used.

The core of the HMT7748 device is supplied by the 3.3V regulator, and thus an external blocking capacitor C_{V3V3} for stable operation is required and is mandatory.

A maximum static load, equivalent to a resistor R_{START_MIN}, may be drawn externally on V3V3 during start-up. A static load is the current which would be drawn continuously by the application circuit if the output voltage, V_{SNS}, were held at a fixed level. A load in excess of this level may block the start-up.

A higher dynamic load (eg. capacitor charging) is permitted. Dynamic loads will affect (slow) the start, but will not block start-up.

In normal operation the consumption of the HMT7748 itself is limited to the quiescent current, I_{QUIES}. During startup, the static load contributed by the HMT7748 on the supply is limited to I_{QUIES_START}. The actual load is increased by the current drawn to charge the application capacitors and any external loads.

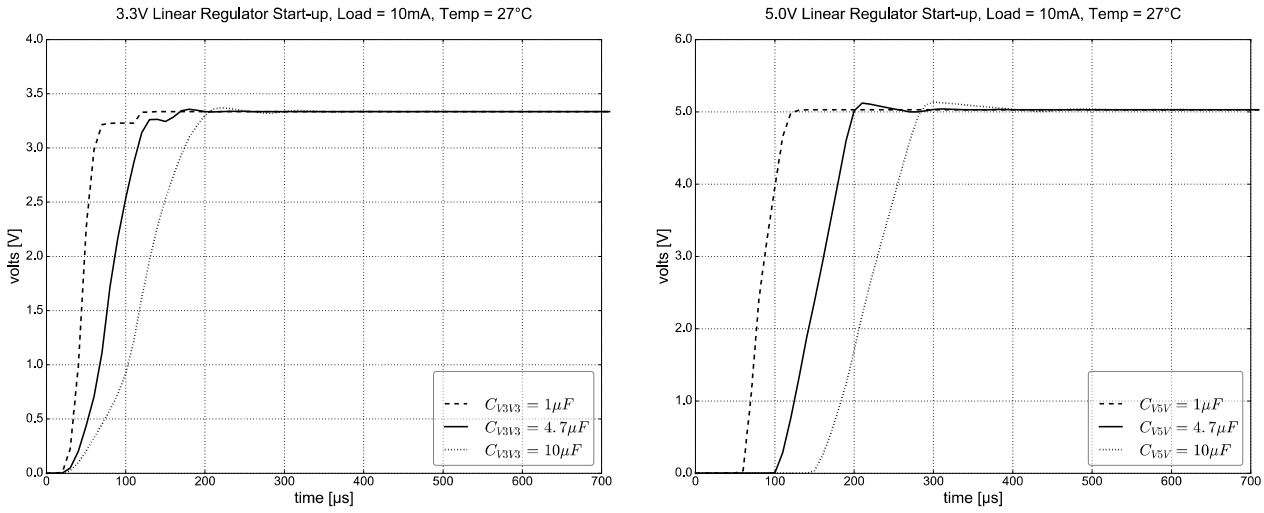


Fig. 15: HMT7748 linear regulators' start-up under different conditions of load capacitance

The 5.0V regulator output is not used internally and is provided for external use. When in use, an external blocking capacitor C_{V5V} must be provided for stable operation, and the input supply range must be sufficient (VPLUS>V_{SUP} in

pure linear mode or VDCDC>$V_{DCDC\_5V\_MIN}$ for DCDC operation).

When the 5.0V linear regulator is not in use, either permanently or periodically, then this block may be placed in a power-down state by setting bit CFG:PD5V. When this bit is set to '1', the 5.0V regulator is placed in power-down and the output pin, V5V, is pulled low with a discharge current of I_{PD5V}. This ensures capacitances on the line are discharged cleanly, and that the output is tied to a known state.

18 Power dissipation

The maximum average power consumption per channel in short circuit is:

$$\frac{max(I_{SAT}).max(V_{PLUS}).t_{SHORT}.N_{RETRY}}{t_{RESTART}} = 26.5\text{mW}$$

The power dissipation into an inductive load, assuming no internal losses in the inductor itself is $f\frac{1}{2}LI^2$,where *f* is the switching frequency, *L* the load inductance and *I* the operating current. The design of the application hardware should take account of this heating.

Fig. 16 shows the means to estimate the device junction temperatures based on the dissipation of the regulator and switches.

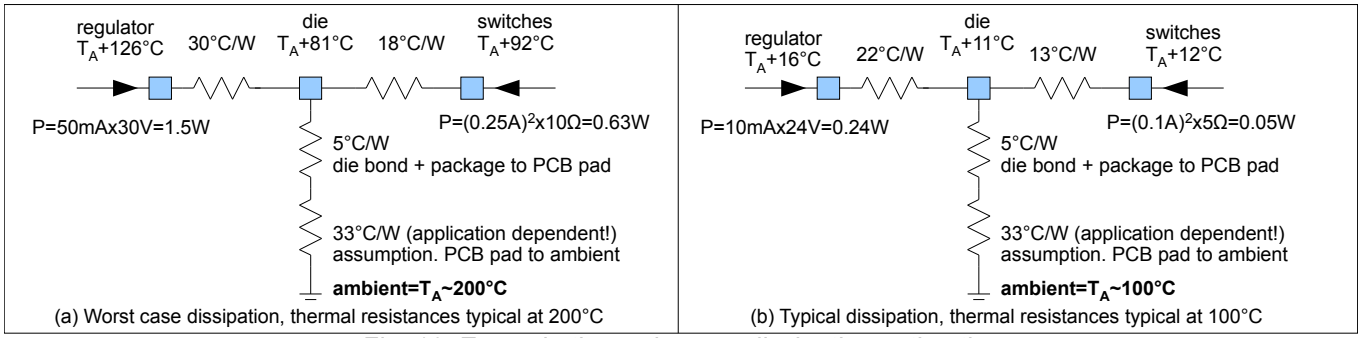


Fig. 16: Example thermal power dissipation estimation

19 Power supply rejection ratio

Fig. 17 shows the measured power supply rejection ratios for various output capacitances and load currents. A DC bias condition of 24V, and typical power supply injected noise levels of 250mVrms were used.

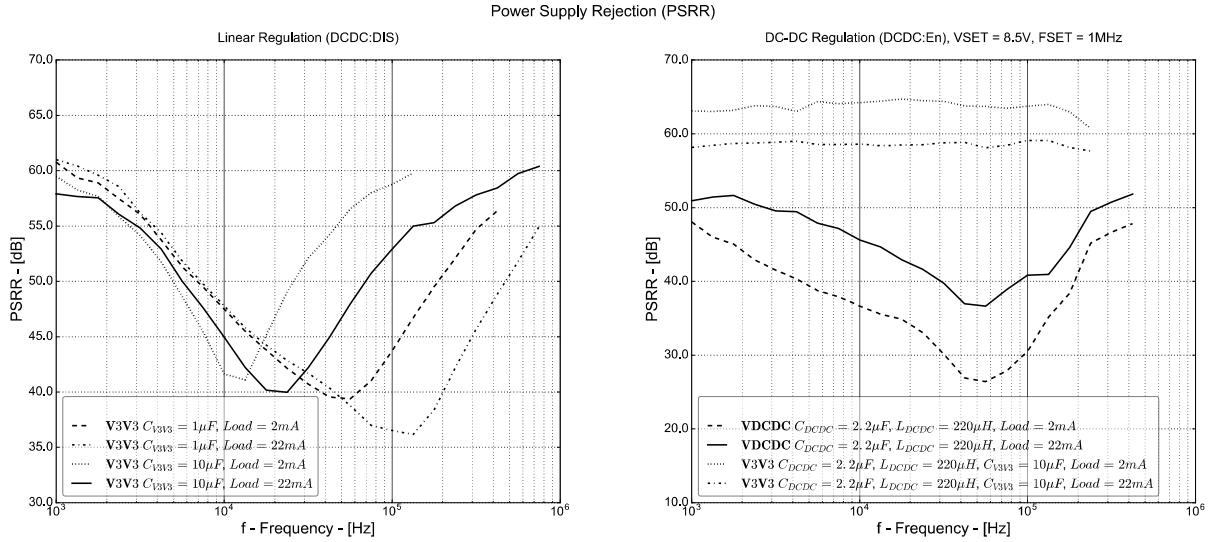


Fig. 17: Power supply rejection ratio under different conditions of C_{V3V3} and I_{V3V3}

20 Output protection and reverse polarisation

The PGND, CQ, DIO and VPLUS pins are fully protected by a surge protection, to withstand an asymmetric surge between any pair of these pins according to IEC 60255-5, i.e. 2A for a half-time of 50µs. Note that the surge stimulus is applied between the pins, rather than in common mode. This subjects the device under test to the current ratings shown in Fig. 18.

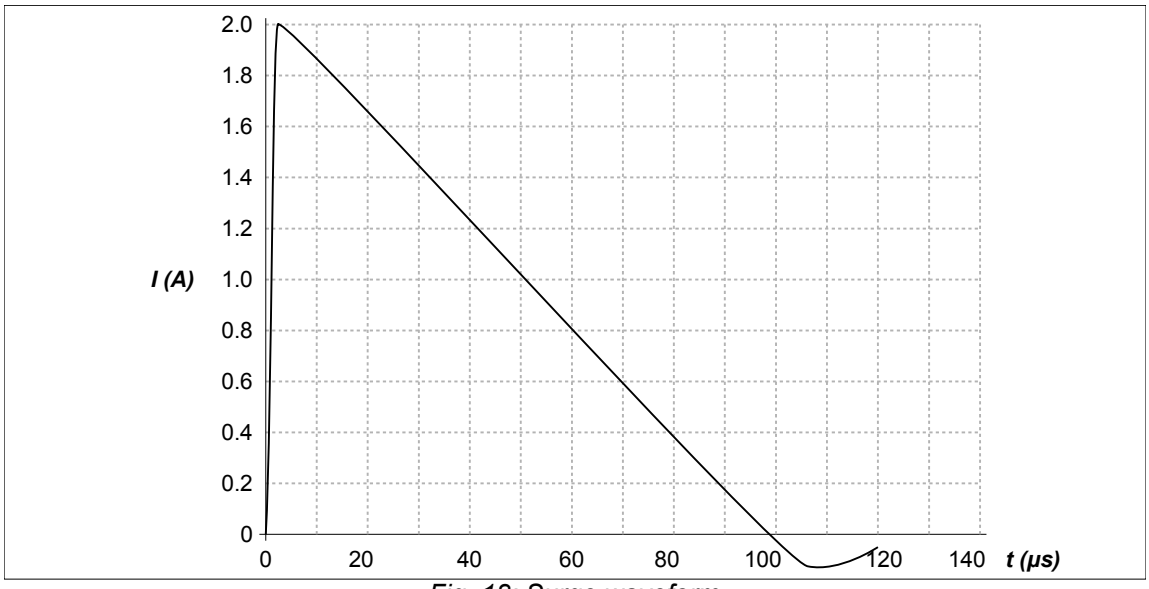


Fig. 18: Surge waveform

The surge protection provides a zener like action with a protection threshold of V_{PROT}, deliberately chosen to be in excess of the normal operating voltages of the HMT7748. Once the surge disturbance is complete, the line voltages recover to normal levels and the zener protection automatically ceases to conduct. This protection style is preferred over an active snap-back protection which may continue to conduct when the operating voltages return to their nominal conditions.

Further external surge protections are compatible with the internal protections where compliance to standards exceeding the demands of IEC 60255-5 are required.

Reverse polarisation protection is included in the HMT7748. When V3V3 is not supplied (V(VPLUS)≤V(PGND)) minimal currents, I_{REV_POL}, will flow between any pair of the pins, up to a maximum voltage difference between any pair of pins of 35V.

Note: if the HMT7748 is rapidly switched from a correctly polarised condition to a reverse polarised condition, such that the C_{V3V3} capacitor remains charged, then the active zener function of the CQ or DIO output will cause a destructive current to flow. Sufficient time should be allowed (ms) during testing of the reverse polarisation function to allow C_{V3V3} to discharge.

21 Register Map

Reg	Addr	Bits	Function
MSEQ	00h	R/W R/W R/W R/W R/W R/W R/W R/W OD1[1:0] | M2CNT[3:0] | OD2[1:0]	OD1[1:0]: 00 backwards compatibility only (type 1) 01 2 octets on-demand data 10 8 octets on-demand data 11 reserved OD2[1:0]: 00 1 octet on-demand data (type 2) 01 2 octets on-demand data 10 8 octets on-demand data 11 reserved M2CNT[3:0] expected octet count on read operation
CFG	01h	R/W R/W R/W R/W R/W R/W R R UVT[2:0] | BD | RF | PD5V | 0 | 0	UVT[2:0]: under-voltage threshold, see §11 BD: 0 baud rate 38.4kbaud 1 baud rate 230.4kbaud RF: 0 absolute CQ/DIO comparator ref. level 1 CQ/DIO comparator ref. level at VPLUS/2

Reg	Addr	Bits	Function
			PD5V: 0 5V regulator active 1 5V regulator inactive
CCTL	02h	R/W R/W R/W R/W R/W R/W R/W R/W TRNS | SCT[2:0] | SGL | SIO | HS | LS	TRNS: set transparent operation mode SCT: short-circuit threshold, see §9 SGL: Single octet UART mode SIO: SIO mode requested HS: enables CQ HS switch LS: enables CQ LS switch
DCTL	03h	R/W R/W R/W R/W R/W R/W R/W R/W EXT | SCT[2:0] | IEN | DIO | HS | LS	EXT: enable use of CTLD pin SCT: short-circuit threshold, see §9 IEN: Level change interrupt enable DIO: DIO mode requested HS: enables DIO HS switch LS: enables DIO LS switch
LINK	04h	R R R/W R/W R/W R/W W W 0 | 0 | CNT[3:0] | END | SND	CNT[3:0]: data buffer fill count * END: Writing '1' declines sending response SND: Writing '1' sends IO-Link response
THERM	05h	R/W R R R/W R/W R/W R/W R/W AUT | 0 | 0 | TH[4:0]	TH[4:0]: Sets thermal shutdown level AUT: 0 automatic thermal control on 1 automatic thermal control off
TEMP	06h	R R R R R R R R 0 | TEMP[6:0]	TEMP[6:0]: current measured temperature value
LED	07h	R/W R/W R/W R/W R/W R/W R/W R/W LED1[3:0] | LED2[3:0]	LED1[3:0]: LED1 control current setting LED2[3:0]: LED2 control current setting
DCDC	08h	R/W R/W R/W R/W R/W R/W R/W R/W DIS | BYP | FSET[2:0] | VSET[2:0]	DIS: Disable DC-DC converter BYP: BYPASS DC-DC converter VSET[2:0]: Set DC-DC converter output voltage FSET[2:0]: Set DC-DC converter operating frequency
DSTAT	09h	R R R R R R R R 1 | 0 | 0 | 0 | 0 | LVL | SSC | 0	LVL: DIO line level SSC: Short-circuit
STATUS	0Ah	R/W R R R R R R R R RST | INT | UV | DINT | CHK | DAT | SSC | SOT	RST: low following reset, set by writing INT: set when interrupt active prior to SPI read UV: under-voltage DINT: DIO interrupt CHK: bad checksum or parity DAT: data available or IO machine is waiting to transmit SSC: short-circuit SOT: over-temperature
FR0-FR14	10h-1eh	R/W R/W R/W R/W R/W R/W R/W R/W DATA[7:0]	15 octet data buffer †

Table 18: Register map

* Valid CNT data may only be read when data is available (DAT bit set). If this is true, then reading the field returns the number received octets.

Writing the CNT field sets the number of octets to transmit. Note that a read back will continue to read the number of octets in the received frame, and not the value written over SPI.

† The data buffer registers are only accessible when frame data is available (DAT bit set).

The initial value of all register bits following reset is '0', except bits DCDC:VSET[2:0], where the default value is 5.

22 Detailed block diagram

Fig. 19 shows the details of the internal blocks of the HMT7748, and indicates which blocks the register fields act on, or are generated by.

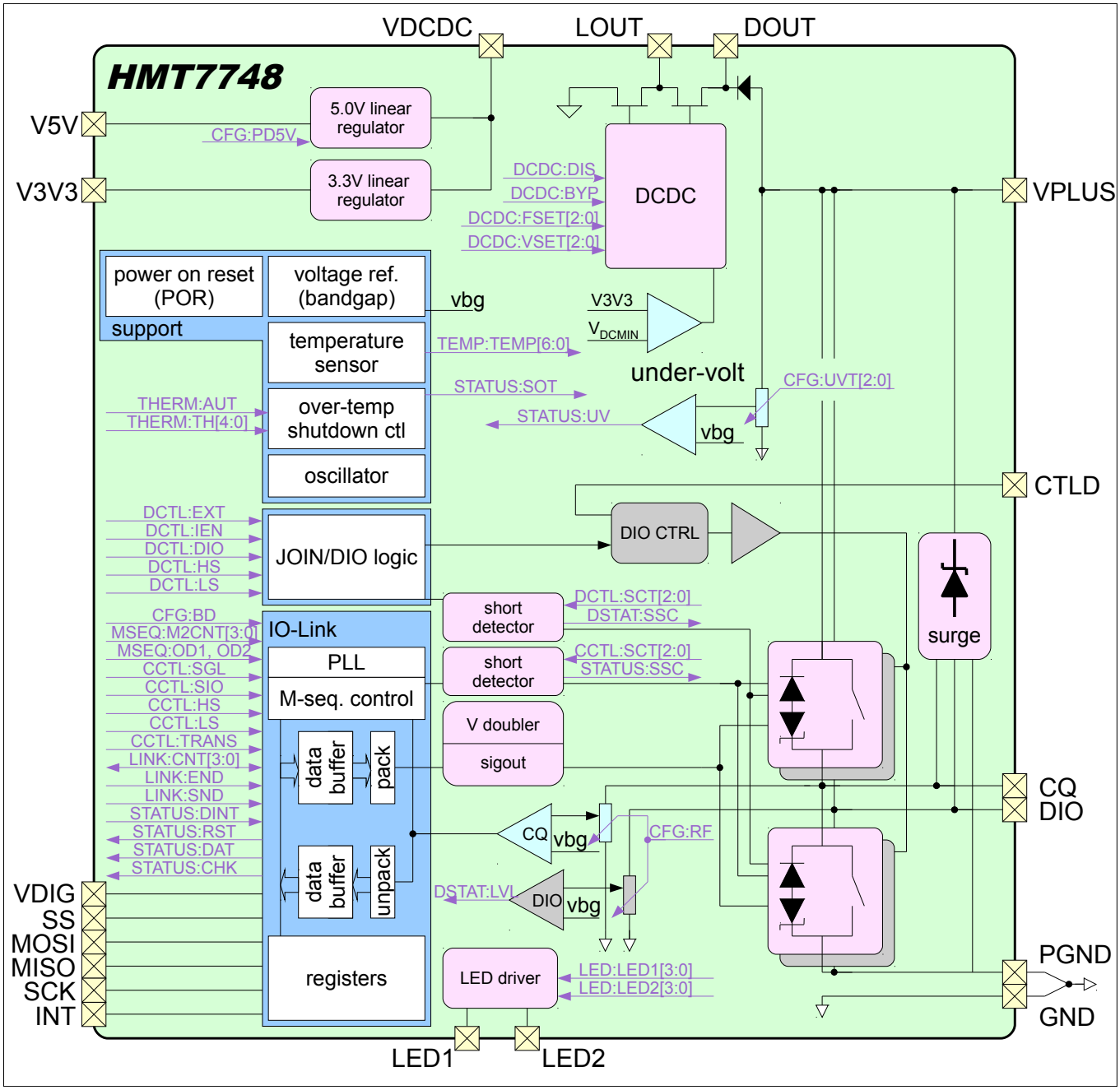


Fig. 19 Detailed block diagram, showing register field connections

23 Pins

Group/Exposure	Description	Pins	V tolerance (2) [V]	Type (1)
Line/External	Line supply voltage	VPLUS	35	PWR
	Line data signal SIO/SDCI	CQ	35	ANA IO
	Line data signal DI/DO	DIO	35	ANA IO
	Switch ground return	PGND	0.7	PWR

Group/Exposure	Description	Pins	V tolerance (2) [V]	Type (1)
	Ground	GND	ref	PWR
SPI/Internal	SPI data, microcontroller to HMT7748	MOSI	5.5	CI
	SPI synchronisation, slave select	SS	5.5	CI
	SPI interface clock signal	SCK	5.5	CI
	SPI data, HMT7748 to microcontroller	MISO	5.5	COZ
	interrupt	INT	5.5	CO
	SPI interface supply	VDIG	5.5	PWR
LED/External	LED1 source current	LED1	5.5	ANA O
	LED2 source current	LED2	5.5	ANA O
Low volt supply/Internal	Sensor and microcontroller supply	V5V	5.5	PWR
		V3V3	3.6	PWR
DCDC/Internal	VPLUS following diode protections	DOUT	35	ANA IO
	Inductor power feed	LOUT	35	ANA IO
	DCDC supply output, intermediate supply	VDCDC	35	PWR
Unused/Internal	Not connected	NC (1off)	-	-
Note 1) PWR: power, CI: CMOS input, CO: CMOS output, COZ: output with tristate function, ANA IO: Analogue input output, ANA O: Analogue output, SIO: Single Input/Output, 2) Indicative only, refer to technical data (§24) for specification limits				

Table 19: HMT7748 pins

24 Technical Data

24.1 Absolute maximum ratings

All values refer to GND unless otherwise specified	Symbol	Min	Max	Unit
Pin voltage VPLUS		-40	40	V
Pin voltage CQ		-40	40	V
Pin voltage DIO		-40	40	V
Pin voltage V3V3		-1	5	V
Pin voltage V5V		-1	7	V
Pin voltage digital pins, LED pins		-1	7	V
Storage temperature range	T_{STOR}	-25	100	°C
Electrostatic protection (HBM 100pF, 1.5kΩ) all pins.	V_{ESD}		4	kV
Soldering temp. (20-40sec, cf. JEDEC J-STD-020C)	T_{LEAD}		260	°C

Table 20: Absolute maximum ratings

Operation above the absolute maximum ratings may lead to instantaneous device failure. Operation of the HMT7748 between the operating ratings and the absolute maximum ratings leads to a reduced operating life-time.

24.2 Operating parameters

	Symbol	Min	Typ	Max	Unit
Operating current supply, no pin currents, DCDC enabled	I_{QUIES}		3.0	3.5	mA
Operating current supply on pin VPLUS during startup	I_{QUIES_START}			10	mA
Junction temperature	T_{MAX}	-40		150	°C
Junction temperature QFN package *	T_{MAX}	-40		150	°C
VPLUS supply voltage, I_{V3V3}=50mA (DCDC disabled)	V_{SUP}	4.5	24	35	V
VPLUS supply voltage, I_{V5V0}=50mA (DCDC disabled)	V_{SUP}	6.5	24	35	V
minimum VPLUS (DCDC enabled) (see Fig. 13)	V_{SUP}		10.5		V
Minimum VDCDC output voltage (V_{SET}) for use of V5V	$V_{DCDC\_5V\_MIN}$	7.5			V
Blocking capacitor on VPLUS	C_{BLK}	100			nF
EMC blocking capacitor	C_{EMC}		470		pF
Capacitor C_{V3V3}	C_{V3V3}	1		10	µF
Capacitor C_{V5V} (V5V in use)	C_{V5V}	1		10	µF
Capacitor C_{DOUT}	C_{DOUT}	10			nF
Capacitor C_{DCDC}	C_{DCDC}		2.2		µF
Capacitor L_{DCDC}	L_{DCDC}		220		µH
Maximum load capacitor CQ (see Fig. 3) **	CQ_{LOAD_MAX}			250	nF
Maximum load capacitor DIO(see Fig. 3) **	DIO_{LOAD_MAX}			250	nF
Maximum load capacitor JOIN mode (see Fig. 4) **	$JOIN_{LOAD\_MAX}$			500	nF
Maximum load inductance CQ (see Fig. 3)	CQ_{LOAD_MAX}			††	mH
Maximum load inductance DIO (see Fig. 3)	DIO_{LOAD_MAX}			††	mH
Maximum load inductance JOIN mode (see Fig. 4)	$JOIN_{LOAD\_MAX}$			††	mH
Thermal resistance to ambient of QFN 20-LD package mounted on a 4-layer PCB, with thermal flag.	Θ_{JA}		38†		°C/W
*in qualification **values measured with pure capacitive load † average die surface temperature, see section 18 for further details †† unlimited, see section 18 for further details.					

Table 21: Operating parameters

24.3 Electrical parameters

Electrical parameters are valid over the operating temperature and voltage range, unless otherwise stated.

Parameter	Conditions, comment	Symbol	Min	Typ	Max	Unit
Receiver CQ/DIO						
Input threshold “H”	RF=0	V_{THH}	10.5		13	V
Input threshold “L”	RF=0	V_{THL}	8		11.5	V
Input threshold “H”	RF=1	V_{THHR}	-10%	V_{PLUS}/2-0.5	+10%	V
Input threshold “L”	RF=1	V_{THLR}	-10%	V_{PLUS}/2+0.5	-10%	V
Hysteresis		V_{HYS}	0.5	1.0	1.5	V
Input range CQ/DIO		V_{IN}	-10		VPLUS+10	V
Noise suppression time		t_{ND}		1/(16.f_{BIT})		µs

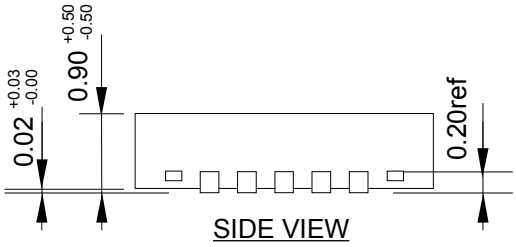
Parameter	Conditions, comment	Symbol	Min	Typ	Max	Unit
Data rate	BD=0	f_{BIT}		38.4		kBaud
Data rate	BD=1	f_{BIT}		230.4		kBaud
Bit time		T_{BIT}		$1/f_{BIT}$		µs
Internal clock base		f_{CK}	-10%	10	+10%	MHz
PLL resolution		f_{RES}		0.4		%
PLL clock stability	change over 2ms	f_{STAB}			1	%
Short circuit and Wake-up detection						
Set current tolerance	see Table 14	I_{SHORT}	-20%	I_{SET}	+20%	mA
Filter delay		t_{SHORT}	-10%	14	+10%	µs
Retries	SIO=1	N_{RETRY}		2		
Retry delay	SIO=1	t_{RETRY}	-10%	50	+10%	µs
Short circuit restart time	SIO=1	$t_{RESTART}$	-10%	100	+10%	ms
POR						
POR release threshold		V_{POR}	1.6	2	2.5	V
POR hysteresis		V_{HYST}		0.1		V
Output switches individual channels CQ/DIO						
Output resistance	I_{OUT}=100mA	R_{SW}			10	Ω
Switching time	C_{LOAD} < 3nF, 10%-90%	t_{SW}			1	µs
Zener voltage	I_{OUT}=100mA	V_{ZEN}	6		10	V
Saturated current		I_{SAT}	0.65	1.2	1.5	A
Line surge protection, parameters with respect to any pair PGND, CQ, DIO, VPLUS						
Protection leakage	V=±35V	I_{PROTLK}			40	µA
Protection threshold	I=0.5A	V_{PROT}	35	40	45	V
Thermal shutdown						
Temperature accuracy	150°C 6σ	ε_T	-10		10	°C
Temperature accuracy	25°C	ε_T	-5		5	°C
Thermal hysteresis		Θ_{HYST}		10		°C
Digital pins (see Fig. 5)						
Output pin current	ΔV=0.5V	I_{DIG}	4			mA
Input low signal		V_{DL}	-0.5		$0.15V_{DIG}$	V
Input high signal		V_{DH}	$0.5V_{DIG}$		V_{DIG}+0.5	V
Clock low phase	SCK	t_{cl}	50			ns
Clock high phase	SCK	t_{ch}	50			ns
Setup wrt. SCK	MOSI	t_{ms}	10			ns
Hold wrt. SCK	MOSI	t_{mh}	10			ns
Setup wrt. SCK	SS	t_{ss}	10			ns
Hold wrt. SCK	SS	t_{sh}	10			ns
Output availability	MISO	t_{md}		18	40	ns
Pull-up resistance	SS, SCK, MOSI	R_{PU}	50		200	kΩ
Pull-down resistance	CTLD	R_{PD}	50		200	kΩ
LED Driver						

Parameter	Conditions, comment	Symbol	Min	Typ	Max	Unit
Sink current base unit	see Fig. 12	I_{LED}	-10%	0.5	+10%	mA
Voltage range		V_{LED}	0.6		V_{V5V}	V
Linear regulators						
Power fail reverse leak		$I_{PLUSREV}$			10	µA
Regulator output capability	V3V3 or V5V	I_{OUT}	50			mA
Startup static capability		R_{START_MIN}	67			Ω
Regulator output voltage	V3V3 0mA<I_{OUT}<50mA	V_{V3V3}	3.0	3.3	3.6	V
Regulator output voltage	V5V 0mA<I_{OUT}<50mA	V_{V5V}	4.5	5.0	5.5	V
PSRR ††		PSRR		98		dB
Pin V5V pull-down current		I_{PD5V}	50	100	200	µA
Under-voltage detect	see Table 15, V_{UV}<10V	V_{UV}	UV_{SET}-1	UV_{SET}	UV_{SET}+1	V
	V_{UV}≥10V	V_{UV}	UV_{SET}-10%	UV_{SET}	UV_{SET}+10%	V
DCDC supply						
V_{SET} tolerance		$\|V_{SET\_TOL}\|$			10%.V_{SET_NOM}	V
V_{SET} step size		t_{VSET}		52		µs
V_{SET} range delay	$V_{SET\_MIN} \rightleftarrows V_{SET\_MAX}$	Δt_{VSET}	7*t_{VSET_MIN}		7*t_{VSET_MAX}	µs
o/p voltage load regulation	0-50mA	R_{DCDC}			2	Ω
o/p voltage transient deviation	* V_{DIST}	V_{DCDC}	-0.5		0.5	V
o/p voltage, start-up	transient overshoot	V_{OVER}			1	V
Recovery time to steady state		T_{SETTLE}			1	ms
Start time to steady state		T_{START}		1		ms
Time to SLEEP state	DCDC:DIS set	$T_{DCSLEEP}$		1		µs
Time to enable BYPASS state	DCDC:BYP bit set	T_{BYP_EN}		1		µs
Time to disable BYPASS state	DCDC:BYP bit cleared	T_{BYP_DIS}		40		µs
Voltage ripple (pk-pk)	†	V_{RIPPLE}			10	mV
Inductor current ripple (pk-pk)	†	I_{ripple}	9	11	14	mA
Minimum V3V3 for VDCDC		V_{DCMIN}	2.8			V
Current at start-up	pin VPLUS.See § 16.4.1	$I_{STARTUP}$	50	70	90	mA
Voltage at start-up	pin VDCDC. See § 16.4.1	$V_{STARTUP}$	7.5	8	8.5	V
Operating frequency		f_{DCDC}	-10%	f_{SET}	+10%	kHz
Efficiency (load > 30mA)	†	η	60	90		%
High side resistance		R_{HIGH}	3.3	6.6	20	Ω
Low side resistance		R_{LOW}	4.5	7.2	20	Ω
Output current		I_{OUT}	0		50	mA
I_{LIMIT} in inductor		I_{LIMIT}	70		80	mA
T_{LIMIT}		T_{LIMIT}		formula		V
Sense resistance		R_{DCPLUS}	0.6	1	1.5	Ω

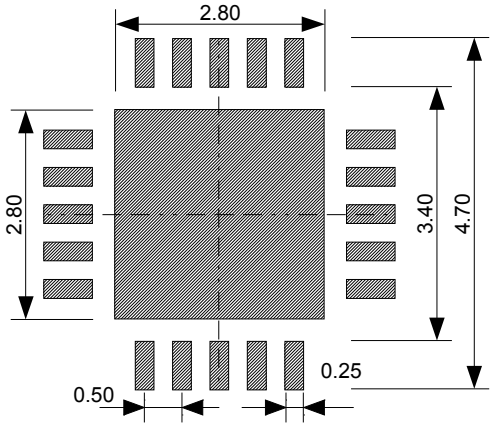
* load current step 10mA to 50mA (or reverse), Input voltage from 10V to 35V (or reverse)
† C_{DCDC}=2.2µF, f_{SET}=1MHz, I_{LOAD}=20mA, L_{DCDC} = 220µH
†† DC at VPLUS=V3V3+2.7V, I_{V3V3}=10mA

Table 22: Electrical parameters

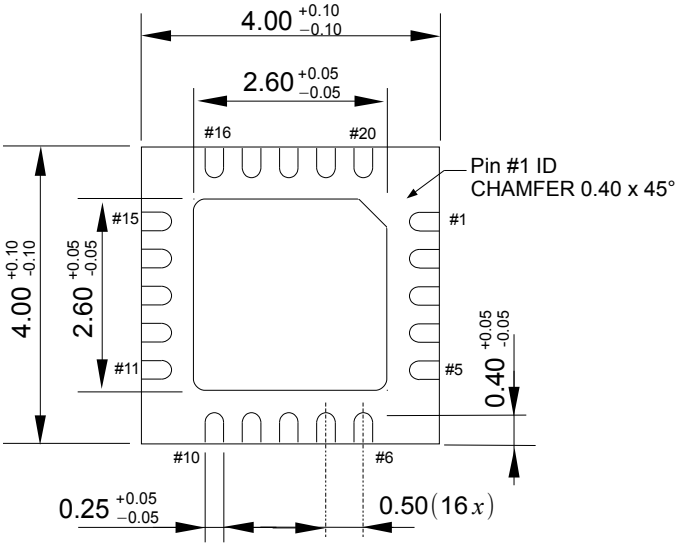
25 Package and footprint drawings



SIDE VIEW



†† FOOTPRINT



BOTTOM VIEW

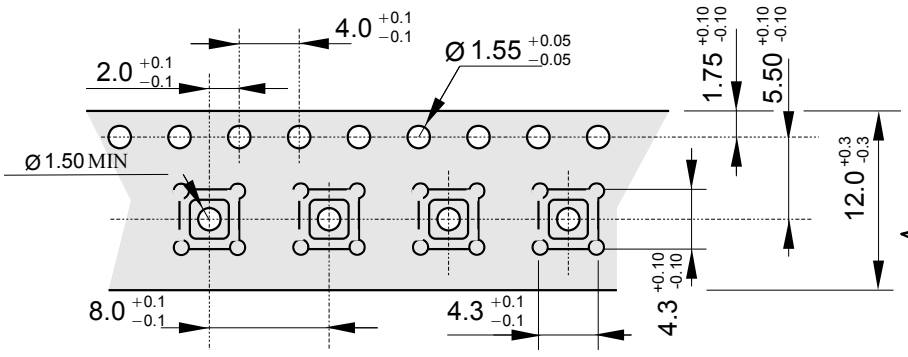
YY: Year code
WW: Week code
L: Lot in week
R: Revision digit

STAMPING TOP VIEW

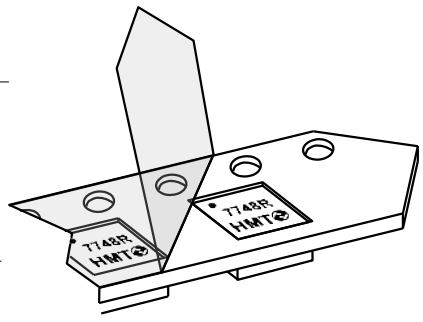
NOTES:

All measurement units are in millimeters

†† Suggested footprint for high density PCB design. Multiple vias from flag to extended internal plane required for correct thermal performance.



Cumulative tolerance of 10 sprocket holes is ±0.2



orientation and feed direction for devices with revision code 3 and up

Fig. 20 Package, footprint and tape drawings

This datasheet is applicable to HMT7748 devices with revision digits 2 & 3